INTEGRATORS' MANUAL

GR64 GSM/GPRS Wireless CPU®

Reference: **WI_DEV_GR64_UGD_001**

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Revision History

Edition	Change Information
First	First Edition
Second	Updated FCC marking requirements Signal connectivity table updated Modified description of UART1 signal behaviour
Third	Review comment implementations
Fourth	Implemented review comments, "Wireless CPU®®" registered signs

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1 Introduction

1.1 Target Users

The GR64 Wireless CPU®s are designed to be integrated into machine-to-machine or man-to-machine communications applications.

They are intended to be used by manufacturers, system integrators, applications developers and developers of wireless communications equipment.

1.2 Prerequisites

It is assumed that the person integrating the Wireless CPU® into an application has a basic understanding of the following:

- GSM networking;
- Wireless communication and antennas (aerials)
- AT commands
- ITU-T standard V.24/V.28
- Micro controllers and programming
- Electronic hardware design

1.3 Manual Structure

This manual is composed of three parts.

Part 1– Overview

This section provides a broad overview of the Gx64 family and includes a list of abbreviations used in the manual.

Part 2 – Integrating the Wireless CPU®

This section describes each of the signals available on the GR64 Wireless CPU®, along with mechanical information. The section also provides the integrator with design guidelines and what is needed to commercialize an application from a regulatory point of view.

Part 3 – Developer's Kit

This section lists the contents of the Developer's Kit and provides the information to setup and use the equipment.

1.4 Notation

The following symbols and admonition notation are used to draw the reader's attention to notable or crucially-important information.

NOTE	**Note** Draws the readers attention to pertinent, useful or interesting information
TIP	**Tip** Provides advice, suggestions, guidance or recommendations which augment the formal text
CAUTION	**Caution** Cautionary information must be heeded, it draws the readers attention to the need for understanding, care or watchfulness in relation to the information provided
WARNING	**Warning** Notes marked warning must be heeded, they alert readers to precautionary measures, risks, hazards or safety information which directly effects equipment function, warranty or personnel safety
DANGER	**Danger** This information must be heeded, it identifies information and cautionary behaviour that otherwise ignored could result in catastrophic equipment failure, bodily injury or death

1.5 Abbreviations

Abbreviation	Explanation
AMR	Adaptive Multi Rate
CBM	Cell Broadcast Message
CPS	Charging Power Supply
CSD	Circuit Switched Data
DCE	Data Circuit Terminating Equipment
DTE	Data Terminal Equipment
EA	Embedded Application
EFR	Enhanced Full Rate
EMC	Electro-Magnetic Compatibility
ETSI	European Telecommunication Standards Institute
FR	Full Rate
GPRS	General Packet Radio Service
GPS	Global Positioning System
GSM	Global System for Mobile Communication
HBM	Human Body Model
HR	Half Rate
IDE	Integrated Development Environment
IP	Internet Protocol
ITU-T	International Telecommunication Union - Telecommunications (Standardization Sector)
LDO	Low-Dropout
M2mpower	Wavecom's powerful support environment

Abbreviation	Explanation
ME	Mobile Equipment (Wireless CPU® without SIM card)
MMCX	Micro Miniature Coax
MO	Mobile Originated
MS	Mobile Station (Wireless CPU® with SIM card)
MT	Mobile Terminated
PCM	Pulse Code Modulation
RF	Radio Frequency
RLP	Radio Link Protocol
RTC	Real Time Clock
SIM	Subscriber Identity Module
SMS	Short Message Service
TCP	Transport Control Protocol
UDK	Universal Developers Kit
UDP	User Datagram Protocol

1.6 Acknowledgements

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2   GR64 Wireless CPU®

2.1   About the GR64

The Wavecom Gx64 family of devices are Quad Band GSM/GPRS Wireless CPU®s operating in the GSM 850/900/1800/1900 bands.

These products belong to a new generation of Wavecom Wireless CPU®s, and are intended to be used in machine-to-machine applications and man-to-machine applications. They are used when there is a need to send and receive data (by SMS, CSD, or GPRS), and make voice calls over the GSM network.

The GR64 conforms to the European Union (EU) Restriction of Hazardous Substances (RoHS) directive 2002/95/EC.

The GR64 is available in two hardware variants. Table 1 lists the hardware features for each variant. The device is available in two hardware variants:

- GR64001. No USB interface or an integrated SIM card holder. VREF is an output to the application.

- GR64002. USB interface and an integrated SIM card holder. VREF is on this variant an input from the application.

Table 1: GR64 HW Variants

Variant	VREF	USB	SIM Card Holder
GR64001	Output	No	No
GR64002	Input	Yes	Yes

Each hardware variant comes in two software variants. One software variant is designed to be controlled from a micro-controller situated on the host application. The other software variant offers the option to run applications embedded onto the Wireless CPU® itself. When using the embedded application version the controlling script can be run internal to the Wireless CPU®, with or without the use of an external control.

A typical application, involves a micro-controller and a Wireless CPU®, in which the micro-controller sends AT commands to the Wireless CPU® via an RS232 communications link.

2.2 Wireless CPU® in a Communication System

Figure 1 and Figure 2 illustrate the main blocks of a wireless communication system using the Wireless CPU®. Figure 1 shows the communication system when the script is embedded on the Wireless CPU® and Figure 2 shows the communication system when a micro-controller is used. They also show the communication principles of the system and the interface between the Wireless CPU® and the application. The definitions in the figures, as used elsewhere in this manual, are in accordance with the recommendations of 3GPP TS 27.007.

NOTE — Up-to-date 3GPP TS 27.007 recommendations can be found at the 3rd Generation Partnership Project (3GPP) web site, at: http://www.3gpp.org/

The MS represents the Wireless CPU® and SIM card. The Wireless CPU® excluding SIM card, is known as the ME.

The DTE (data terminal equipment) is the controlling application. This can be either an external host or an internal embedded application.

The DCE (data circuit terminating equipment) is the serial communication interface of the MS.
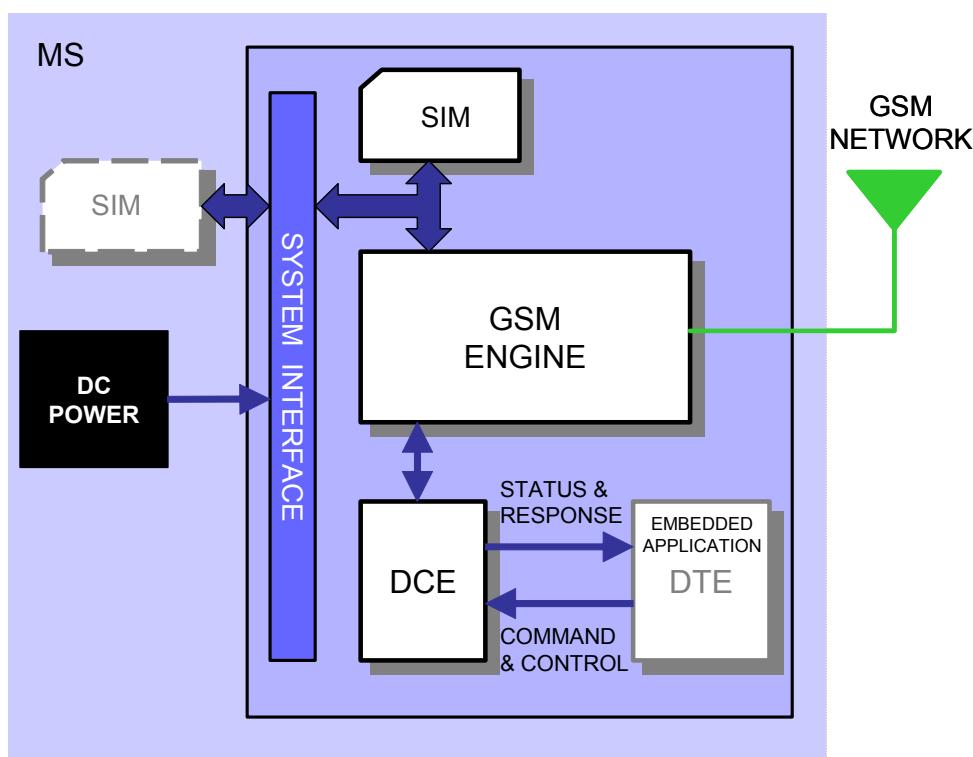
Figure 1: Main Blocks in a Wireless System (embedded application)
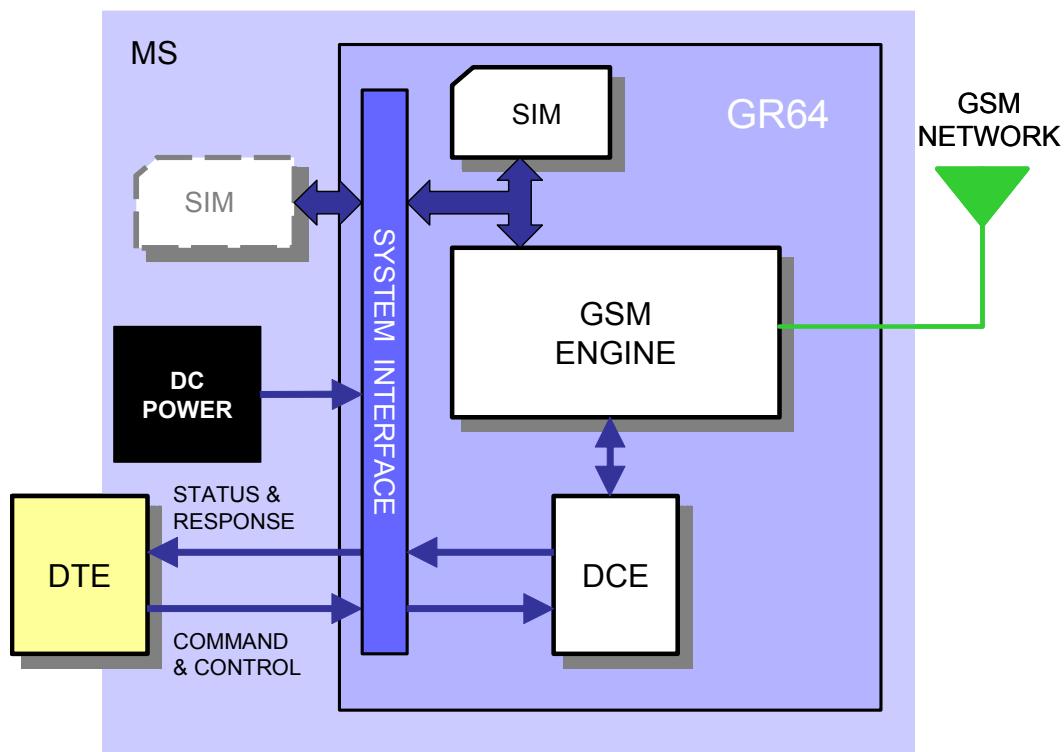
Figure 2: Main Blocks in a Wireless System (external micro-controller)

In accordance with the recommendations of ITU-T (International Telecommunication Union - Telecommunications Standardization Sector) V.24, the TE communicates with the MS over a serial interface.

The functions of the Wireless CPU® follow the recommendations provided by 3GPP (3rd Generation Partnership Project) and ITU-T. 3GPP is a collaboration agreement that was established in December 1998. The collaboration agreement brings together a number of telecommunications standards bodies which are known as *Organizational Partners*. The current Organizational Partners are ARIB, CCSA, ETSI, ATIS, TTA, and TTC.

3GPP specifies a set of AT commands for controlling the GSM element of the Wireless CPU®; these commands are supplemented by Wavecom specific commands.

To find out how to work with AT commands, see the AT Commands Manual.

2.3 Features

The Wireless CPU® performs a set of telecom services (TS) according to 3GPP release 99 and ITU-T. The functions of the Wireless CPU® are implemented by issuing AT commands over a serial interface.

2.3.1 Types of Wireless CPU® Equipment

The GR64 is a fully Quad Band capable GSM/GPRS Wireless CPU® with the characteristics shown in the table below.

Feature		GSM850	E-GSM900	GSM1800	GSM1900
Frequency range (MHz)	Tx	824–849	880–915	1710–1785	1850–1910
	Rx	869–894	925–960	1805–1880	1930–1990
Channel spacing		200kHz	200kHz	200kHz	200kHz
Number of channels		124	174	374	299
Number of TD slots		8	8	8	8
Duplex spacing		45MHz	45MHz	95MHz	80MHz
GSM power class		4 (2W)	4 (2W)	1 (1W)	1 (1W)
Modulation		GMSK			
Receive sensitivity		<–102dBm at antenna connector			
GPRS multi-slot class		Class 10			

2.3.2 Short Message Service

The Wireless CPU® supports the following SMS services:

- Sending; MO (mobile-originated) with both PDU (protocol data unit) and text mode supported
- Receiving; MT (mobile-terminated) with both PDU and text mode supported

- CBM (cell broadcast message); a service in which a message is sent to all subscribers located in one or more specific cells in the GSM network (for example, traffic reports)
- SMS status report according to 3GPP TS 23.40

The maximum length of a text mode SMS message is 160 characters using 7-bit encoding. The Wireless CPU® supports up to six concatenated messages to extend this function. Concatenation is performed by the host application.

2.3.3   Voice Calls

The Wireless CPU® offers the capability of MO (mobile originated) and MT (mobile terminated) voice calls, as well as supporting emergency calls. Multi-party, call waiting and call divert features are available. Some of these features are network-operator specific.

For the inter-connection of audio, the Wireless CPU® offers both single ended and balanced analogue input and output lines. Direct interface to the digital PCM (pulse code modulation) bus used within the Wireless CPU® is available, thus by-passing the internal analogue circuitry. The Wireless CPU®s support HR, FR, EFR and AMR vocoders.

2.3.4   Data

The Wireless CPU® supports the following data protocols:

- GPRS (General Packet Radio Service)
  The Wireless CPU® is a Class B terminal. The Wireless CPU® is GPRS multi-slot class10 (4+2) enabled, capable of receiving at a maximum of four timeslots per frame (down link), and transmitting in two timeslots per frame (up link). See section 2.3.5 for multi-slot allocation by class.
- CSD (Circuit Switched Data)
  The GR64 Wireless CPU® is capable of establishing a CSD communication at 9.6 kbps over the air.

2.3.5   GPRS Multi-Slot Support

GSM Multi-slot classes supported by Gx64 devices

Multi-slot Class	Maximum slot allocation			Allowable Configuration	Max data rate
	Downlink	Uplink	Active		
8	4	1	5	1 up; 4 down	8–12Kbps Send 32–48Kbps Receive
10	4	2	5	1 up; 4 down	8–12Kbps Send 32–48Kbps Receive
				2 up; 3 down	16–24Kbps Send 24–36Kbps Receive

2.3.6   SIM Card

The GR64 supports an external SIM card through its system connector. A variant of the GR64 also supports an on-card SIM. For dual SIM support, automated SIM-switching is available. Both 3V and 1.8V SIM technology is supported. Older, 5V SIM technology is not supported.

A mechanical variant of the GR64 also supports an on-card SIM. For dual SIM support, automated SIM-switching is available. Only one SIM is active at any one time, it is not possible to concurrently register on more than one network.

2.3.7   Power Consumption

Feature		Power Off	Sleep Mode (DRX8)	Idle Mode	Transmit Operation (peak average)
GSM850 & E-GSM900	Voice/CSD	<100uA	1.6 mA	27 mA	2050 mA
	Data/(GPRS)				
GSM1800 & GSM1900	Voice/CSD	<100uA	1.6 mA	27 mA	1450 mA
	Data/(GPRS)				

The power consumption figures shown represent typical average current for maximum transmitted power, single uplink (transmit) slot, and single downlink (receive) slot. The Wireless CPU® will consume more average power in different multi-slot configurations, the worst case being that of two uplink and three downlink slots.

2.3.8   Operating Environment

Parameter	Min	Max	Units
Operating Temperature	−30	+75	℃
Humidity		95	%
Storage Temperature	−40	+85	℃

For complete details of the environmental specification please refer to Section 9.5.

2.3.9   Other Features

The GR64 supports many other features, including:

- 3GPP TS 27.010 multiplexing
- SIM application tool kit, class 2 release 99 compliant
- On board TCP/IP stack

In addition, customers have the option of a GR64 software variant which adds embedded application functionality.

2.4 Service and Support

2.4.1 Web Pages

Visit the Wavecom extranet web site for the following information:

- Where to buy Wireless CPU®s or for recommendations concerning accessories and components
- Local contact details for customer support in the region
- FAQs (frequently asked questions)

Access to the Wavecom extranet site requires a user account and password. Accounts can be arranged through the local account manager.

The extranet web site address is:

http://www.wavecom.com/modules/movie/scenes/support/

2.4.2 AT Commands Manual

The AT Commands Manual provides users with all the AT commands that can be used with the Wireless CPU®. AT commands appear in logical groups and contain the command, a description of its functionality and an example of use.

2.4.3 M2mpower Application Guide

The M2mpower Application Guide provides users with all the information they need to build an application using the M2mpower support environment. This manual is supplied as part of the M2mpower package.

2.4.4 Developer's Kit

Wavecom provides the developer's kit to get the integrator started quickly. The kit includes the following hardware which is required to begin the development of an application:

- This Integrator's Manual
- Developer's kit hardware
- Developer's kit accessories
- Power supply & adapters

- RS232 cable
- Headset
- Antenna: 900 & 1800 MHz
- Antenna: 850 & 1900 MHz

Make sure to order the M2M Wireless CPU®(s) that are applicable to the needs of the organization. Also, ensure that the integrator have computer or micro-controller. The AT command manual provides the necessary command and control reference to drive the Wireless CPU®.

2.5   Precautions

The Wireless CPU®s are ESD protected up to ±15kV on all 2.8V IO pins. All other pins are protected up to ±2kV. Integrators must follow electronic device handling precautions when working with any electronic device system to ensure no damage occurs to the host or the Wireless CPU®. In the section 'Integrating the Wireless CPU®', users will find more information about safety and product care. Do not exceed the environmental and electrical limits as specified in 'Technical Data' section.

2.6   Guidelines for Safe and Efficient Use

Users must follow the general usage outlined in this chapter before using the GR64 for any purpose.

2.6.1   General Usage

- Always treat the product with care and keep it in a clean and dust-free place.
- Do not expose the product to liquid.
- Avoid exposing the product to moisture or high humidity environments.
- Do not expose the product to extreme high or low temperatures beyond those specified for operation and storage.
- Do not expose the product to open flames or lit tobacco products.
- Do not drop, throw or try to bend the product.
- Do not paint the product.
- Do not use the product near medical equipment without requesting permission.
- Do not use the product when in or around aircraft, or areas posted "turn off two-way radio".
- Do not use the product in an area where a potentially explosive atmosphere exists.
- Do not place the product or install wireless equipment in the area above a vehicle's air bag.
- Do not attempt to disassemble the product; only Wavecom authorized personnel should perform servicing.

2.6.2   Radio Frequency (RF) Exposure and SAR

The Wireless CPU® device is a low-power radio transmitter and receiver (transceiver). When it is turned on, it emits low levels of radio frequency energy (also known as radio waves or radio frequency fields).

Governments around the world have adopted comprehensive international safety guidelines, developed by scientific organizations, e.g. ICNIRP (International Commission on Non-Ionizing Radiation Protection) and IEEE (The Institute of Electrical and Electronics Engineers Inc.), through periodic and thorough evaluation of scientific studies. These guidelines establish permitted levels of radio wave exposure for the general population. The levels include a safety margin designed to assure the safety of all persons, regardless of age and health, and to account for any variations in measurements.

Specific Absorption Rate (SAR) is the unit of measurement for the amount of radio frequency energy absorbed by the body when using a transceiver. The SAR value is determined at the highest certified power level in laboratory conditions, but the actual SAR level of the transceiver while operating can be well below this value. This is because the transceiver is designed to use the minimum power required to reach the network.

The GR64 Wireless CPU® device has been approved for applications where the antenna is located >20cm from the body. In all other configurations the integrator is responsible for meeting the local SAR regulations.

Integrators of the GR64 Wireless CPU® device are responsible for ensuring that they meet the SAR regulatory requirements of the countries in which they intend to operate the device, and that their documentation contains the relevant SAR declaration, certification information, and user guidance as appropriate.

2.6.3   Personal Medical Devices

Wireless CPU® devices may affect the operation of cardiac pacemakers, hearing aids and certain other implanted equipment. If a minimum distance of 15 cm (6 inches) is maintained between the GR64 Wireless CPU®'s radiating antenna and a pacemaker, the risk of interference is limited. If the integrator's application is likely to be situated in the vicinity of personnel, a suitable warning should be contained in the equipment manual to this effect.

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2.6.4   Disposal of Old Electronic Equipment

This symbol on the product or on its packaging indicates that this product shall not be treated as household waste. Instead it shall be handed over to an appropriate collection point for the recycling of electrical and electronic equipment. By ensuring this product is disposed of correctly, the integrator will help prevent potential negative consequences for the environment and human health, which could otherwise be caused by inappropriate waste handling of this product. The recycling of materials will help to conserve natural resources. For more detailed information about recycling of this product, please contact the local city office, the household waste disposal service, or the Wavecom regional sales office.

2.7   Product Marking

Attention must be drawn to the Regulatory Notices contained in Section 10, specifically the paragraph pertaining to the FCC marking requirements for devices in which the GR64 is installed. Any device that integrates the GR64, which is subject to FCC regulatory approval, must have an exterior label identifying the GR64 FCC ID number.

INTEGRATING THE

WIRELESS CPU®

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3 Mechanical Description

3.1 Interface Description

The pictures below show the mechanical design of the Wireless CPU® along with the positions of the different connectors and mounting holes. The Wireless CPU® is protected with tin coated steel ASI 1008/1010 covers that meet the environmental and EMC requirements.
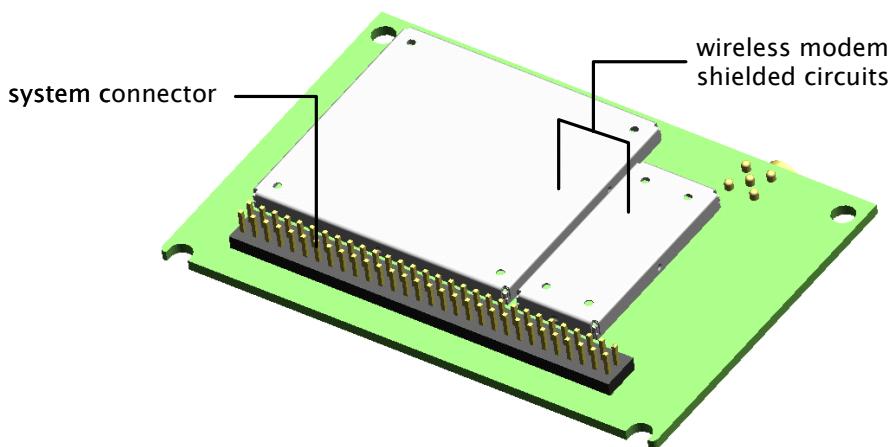
Figure 3: Wireless CPU® viewed from below
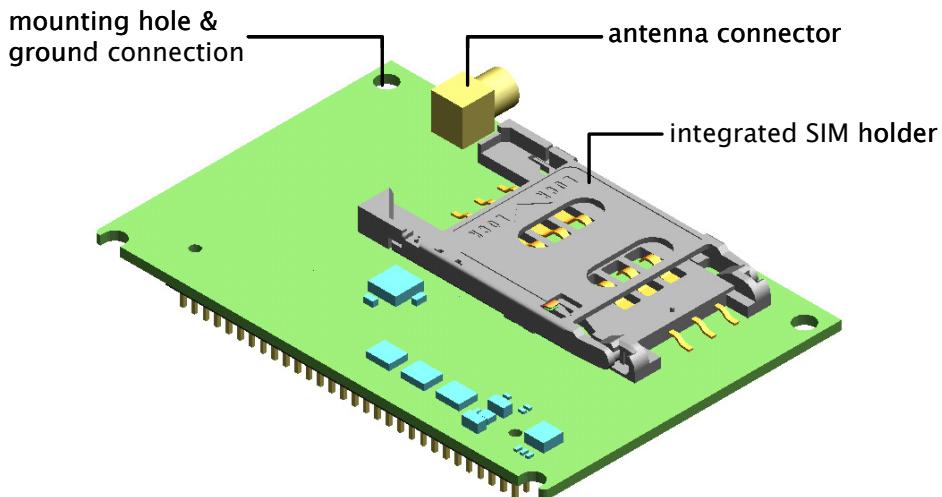
Figure 4: Wireless CPU®, viewed from above (Integrated SIM holder variant)

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Please note the following:

- Mounting holes positioned at the corners make it possible to securely bolt the Wireless CPU® into the application.

- Keypad, display, microphone, speaker and battery are not part of the Wireless CPU®.

- For the GR64 variant without an integrated SIM holder, the SIM card is mounted in the user application, external to the Wireless CPU® (this is also an option for the integrated SIM holder variant).

- The System Connector is a 60-pin standard 0.05 in (1.27 mm) pitch type. The pins and their electrical characteristics are described in Section 5, together with the System Connector Interface.

- Antenna Connector details are found in Section 5.

3.2 Antenna Pad

An antenna pad is available for customers who want to mount a pig-tail antenna onto GR64. The pads (Antenna and Ground) are located on the same side as the system connector (see Figure 5 below).
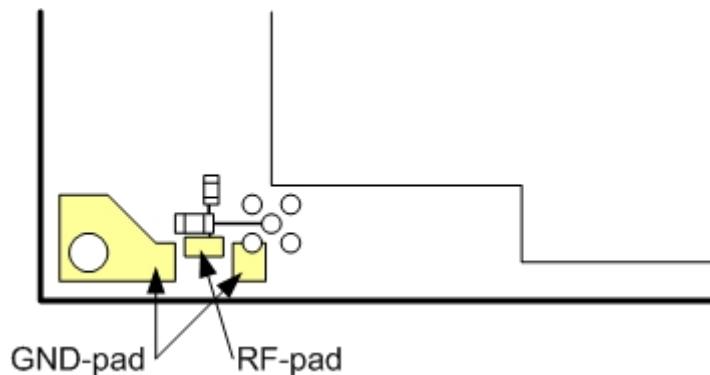
Figure 5: Antenna pig-tail pads

The small pad in the middle is the RF-pad while the larger pads on both sides are ground.

3.3 Physical Dimensions
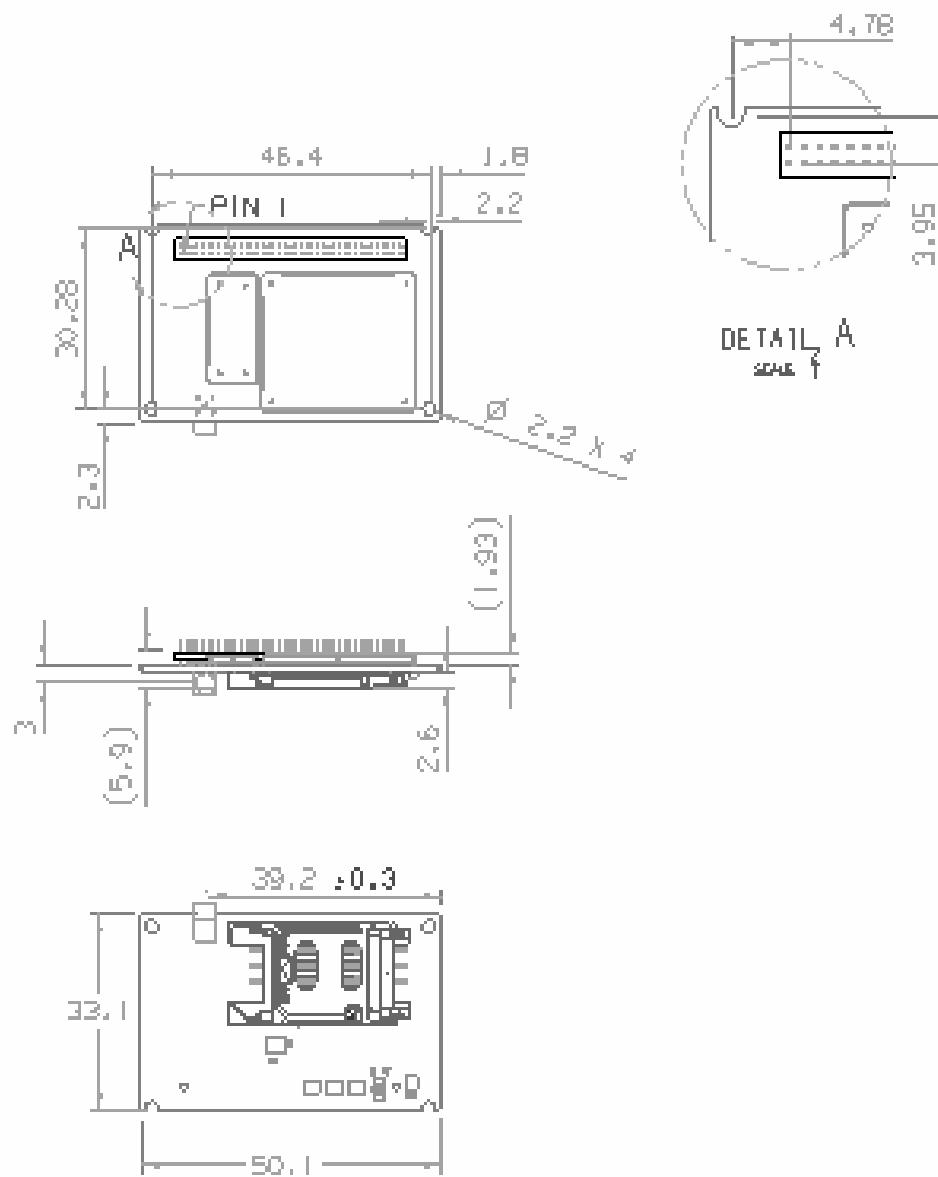
Figure 6: Dimensions of the Wireless CPU® (Integrated SIM variant)

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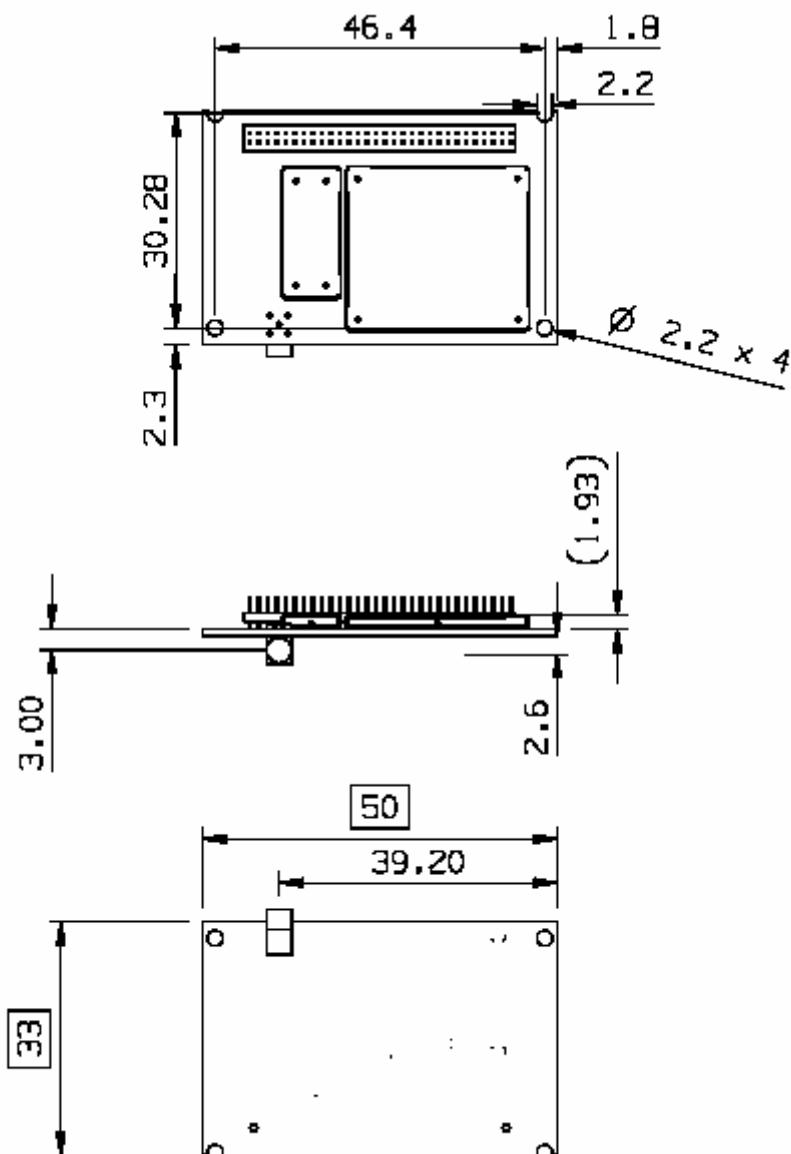
Figure 7: Dimensions of the Wireless CPU® (Legacy variant)

Measurements are given in millimetres. See also Technical Data, in Section 9.

4 System Connector Interface

4.1 Overview

Electrical connections to the Wireless CPU® (except the antenna), are made through the System Connector Interface. The system connector is a 60-pin, standard 0.05 in (1.27 mm) pitch device.

The system connector allows both board-to-board and board-to-cable connections to be made. Use a board-board connector to connect the Wireless CPU® directly to a PCB, and a board-cable connector to connect the radio device via a cable. Surface mount mating connectors for the 60-pin system connector are available from Harwin (part number M50-3113022).

Figure 8 below shows the numbering of the connector pins.

An optional ground connection is provided at the mounting hole next to the RF connector on the Wireless CPU® as shown below. Connect this ground point to the GND pins of the Wireless CPU® by the shortest, low-impedance path possible. The purpose of this connection is to allow for antenna ESD strikes to bypass the Wireless CPU®'s internal ground path.
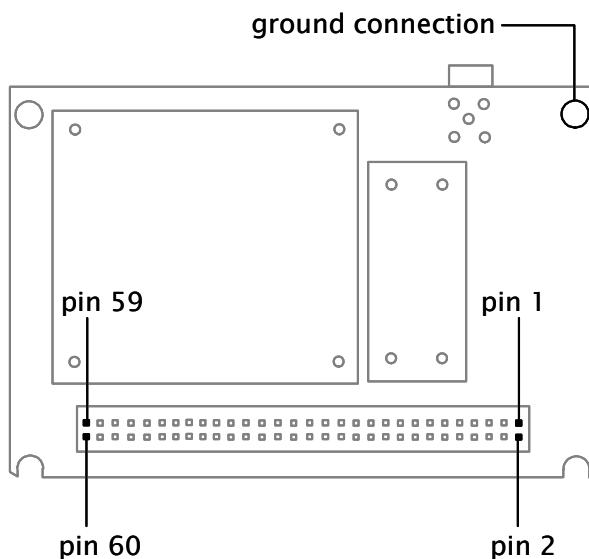
Figure 8: Wireless CPU®, viewed from underneath

The following table gives the pin assignments for the system connector interface and a short description for each signal. The rightmost column indicates whether the signal is required to be used or not.

Table 2: Pin Assignments

Pin	Name	Direction	Function	PIN Req
1	VCC	Input	DC power	Yes
2	GND	–	Ground	Yes
3	VCC	Input	DC power	Yes
4	GND	–	Ground	Yes
5	VCC	Input	DC power	Yes
6	GND	–	Ground	Yes
7	VCC	Input	DC power	Yes
8	GND	–	Ground	Yes
9	VCC	Input	DC power	Yes
10	GND	–	Ground	Yes
11	CHG_IN	Input	Battery charger power	
12	GND	–	Ground	Yes
13	ADIN4	Input	ADC Input 4	
	GPIO5	In/Out	General purpose IO	
14	ON/OFF	Input	Device on/off control	Yes
15	SIMVCC	Output	1.8V or 3.0V SIM card supply	Yes[1]
16	SIMDET	Input	SIM presence detection	Yes[1]
17	SIMRST	Output	SIM card reset signal	Yes[1]
18	SIMDAT	In/Out	SIM card data	Yes[1]
19	SIMCLK	Output	SIM card clock signal	Yes[1]
20	GPIO15	In/Out	General purpose IO	
21	GPIO1	In/Out	General purpose IO	
22	GPIO2	In/Out	General purpose IO	
23	GPIO3	In/Out	General purpose IO	
24	GPIO4	In/Out	General purpose IO	
25	VRTC	Input	DC supply for real time clock	
26	ADIN1	Input	ADC Input 1	
27	ADIN2	Input	ADC Input 2	
28	ADIN3	Input	ADC Input 3	
29	SDA	In/Out	I^{2}C data	
30	SCL	Output	I^{2}C clock signal	
31	BUZZER	Output	Buzzer Output	
32	DSR1	Output	Data Set Ready (UART1)	Yes[2]
	GPIO7	In/Out	General purpose IO	
33	LED	Output	LED control signal	
	GPIO6	In/Out	General purpose IO	
34	VREF	In (Out)	Core voltage reference	Yes

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Pin	Name	Direction	Function	PIN Req
35	TX_ON	Output	Transmit indication	
36	RI	Output	Ring Indicator	
	GPIO8	In/Out	General purpose IO	
37	DTR1	Input	Data Terminal Ready (UART1)	Yes[2]
	GPIO10	In/Out	General purpose IO	
38	DCD1	Output	Data Carrier Detect (UART1)	
	GPIO11	In/Out	General purpose IO	
39	RTS1	Input	Ready To Send (UART1)	Yes[2]
	GPIO9	In/Out	General purpose IO	
40	CTS1	Output	Clear To Send (UART1)	Yes[2]
	GPIO12	In/Out	General purpose IO	
41	DTM1	Input	Data To Wireless CPU® from host (UART1)	Yes[3]
42	DFM1	Output	Data From Wireless CPU® to host (UART1)	Yes[3]
43	DTM3	Input	Data To Wireless CPU® from host (UART3)	
44	DFM3	Output	Data From Wireless CPU® to host (UART3)	
45	USBDP	In/Out	USB data positive	Yes[4]
46	USBDN	In/Out	USB data negative	Yes[4]
47	SSPDTM	Input	Serial PCM data to Wireless CPU® from host	
48	SSPDFM	Output	Serial PCM data from Wireless CPU® to host	
49	VUSB	Input	USB DC power	Yes[4]
50	ALARM	Output	RTC alarm	
51	SSPFS	In/Out	Serial PCM frame synchronization	
52	SSPCLK	In/Out	Serial PCM clock	
53	MICIP	Input	Microphone input positive	
54	MICIN	Input	Microphone input negative	
55	EARP	Output	Earpiece output positive	
56	EARN	Output	Earpiece output negative	
57	AUXO	Output	Auxiliary audio from Wireless CPU® to host	
58	SERVICE	Input	Flash programming enable signal	
59	AUXI	Input	Auxiliary audio to Wireless CPU® from host	
60	AREF	–	Analogue reference	

NOTE

[1] – These signals are required if the external SIM interface is used

[2] – These pin connections are required for sleep mode operation

[3, 4] – At least one of these interfaces is required to be connected

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4.2   Dealing with Unused Pins

Integrators applications may connect all of the GR64 signals pins, or just those necessary for minimal operation, or most commonly some other permutation. If GR64 signal pins are not connected to the host application the integrator should terminate them in the following manner.

Table 3: Unused Pin Termination

Pin	Name	Unused pin termination
1, 3, 5, 7, 9	VCC	Must be connected
2, 4, 6, 8, 10, 12	GND	Must be connected
11	CHG_IN	Leave Open
13	ADIN4/GPIO5	Leave Open
14	ON/OFF	Must be connected
15	SIMVCC	Leave Open
16	SIMDET	Leave Open
17	SIMRST	Leave Open
18	SIMDAT	Leave Open
19	SIMCLK	Leave Open
20	GPIO15	Leave Open
21	GPIO1	Leave Open
22	GPIO2	Leave Open
23	GPIO3	Leave Open
24	GPIO4	Leave Open
25	VRTC	Leave Open
26	ADIN1	Ground
27	ADIN2	Ground
28	ADIN3	Ground
29	SDA	Leave Open
30	SCL	Leave Open
31	BUZZER	Leave Open
32	DSR1/GPIO7	Leave Open
33	LED/GPIO6	Leave Open
34	VREF	Must be connected[1]
35	TX_ON	Leave Open
36	RI/GPIO8	Leave Open

[1] VREF must be used to re-reference the application logic levels to the level used by the GR64, see 4.3.1 and 4.6 for more information.

Pin	Name	Unused pin termination
37	DTR1/GPIO10	Leave Open
38	DCD1/GPIO11	Leave Open
39	RTS1/GPIO9	Leave Open
40	CTS1/GPIO12	Leave Open
41	DTM1	Leave Open
42	DFM1	Leave Open
43	DTM3	Leave Open
44	DFM3	Leave Open
45	USBDP	Leave Open
46	USBDN	Leave Open
47	SSPDTM	Leave Open
48	SSPDFM	Leave Open
49	VUSB	Leave Open
50	ALARM	Leave Open
51	SSPFS	Leave Open
52	SSPCLK	Leave Open
53	MICIP	Connect to AREF
54	MICIN	Connect to AREF
55	EARP	Leave Open
56	EARN	Leave Open
57	AUXO	Leave Open
58	SERVICE	Ground
59	AUXI	Connect to AREF
60	AREF	Leave Open

4.3   General Electrical and Logical Characteristics

The core digital IO is based upon 1.8V technology in the Baseband chipset. All external IO signals undergo bi-directional level shifting on the physical Wireless CPU® to provide flexibility to users of different voltage technology. An internal core IO regulator is used as a reference for the Wireless CPU®-side logic, whilst the application (host-side) reference is fed by VREF in one of two implementations.

In order to provide legacy users a migration path to GR64, the Wireless CPU® IO is made compatible with 2.8V (or level-adapted 3.0V) controllers, popular in older technology applications. This arrangement is implemented in variant product GR64001 and all its SW-variants. In these products the 2.8V VREF is derived from an internal voltage regulator, distributed to the host-side level translators and also output on the VREF signal pin.

The arrangement differs in non-legacy variant GR64 product GR64002 and all its SW-variants. In these products the internal voltage regulator is disconnected and the user application provides the VREF as a reference to the host-side level translators.

The range of VREF voltages is specified in section 4.6.

NOTE	Many of the signals indicated in Table 2 are high-speed CMOS logic inputs or outputs powered by the 1.8V internal core regulators, and then subsequently level shifted at the system interface. All serial interfaces and general purpose IO fall in to this category.

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4.3.1 Level Translator Interfaces

Two different level translator circuits are implemented in GR64. The 'common' interface is used on all level-translated IO with the exception of the I2C signals, SDA & SCL.

4.3.1.1 Common Level Translator Interface

The common level translator used within the GR64 uses a Maxim MAX3001E. The level translators have built-in ESD protection to ±15kV (HBM).
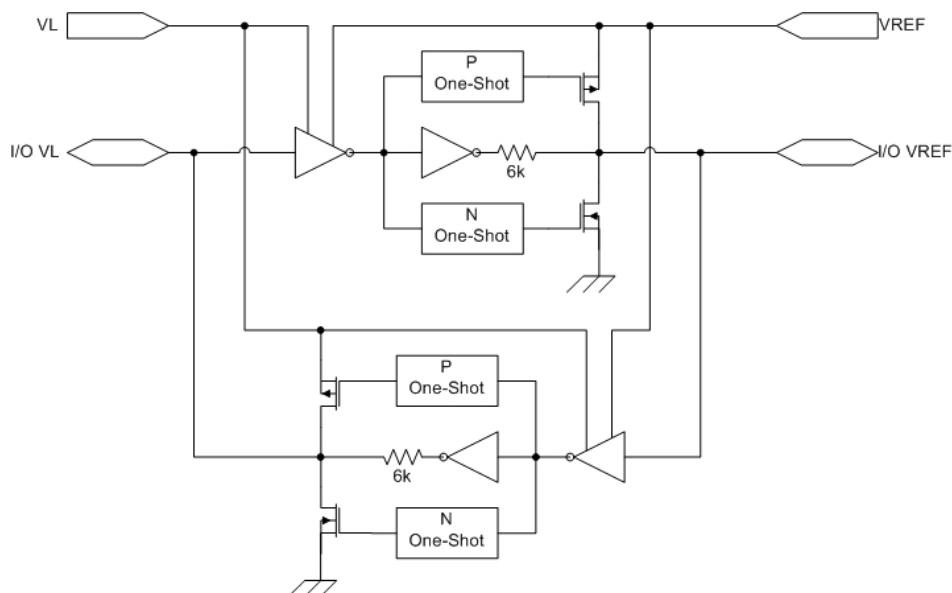
Figure 9: Common level translator circuitry using MAX3001

VREF represents the application side while VL represents the Wireless CPU® side.

Table 4: Level Translator I/O Logic Levels

Parameter	Min	Nom	Max	Unit
IO input voltage high threshold (V_{IHC})	0.75*VREF		VREF	V
IO input voltage low threshold (V_{ILC})	0		0.3	V
IO output voltage high threshold (V_{OHC})	0.67*VREF		VREF	V
IO output voltage low threshold (V_{OLC})	0		0.4	V
Rise and Fall time (C_L = 15pF)			15	ns
IO input impedance (pulled to VREF or GND)		6		kohm

4.3.1.2 I2C Level Translator Interface

Because of the nature of the I2C interface signals, SDA (data) & SCL (clock), they utilize a different type of level-translating technology to that of the 'common' IO. The I2C level translator IC uses an open drain construction with no direction pin, ideally suited to bi-directional low voltage (such as the GR64 1.8 V processor) I2C port translation to the normal 3.3 V or 5.0 V I2C-bus signal levels. Unlike the common level translators, the I2C level translators have a very low (6.5ohm RDSON) resistance between input and output pins.

The I2C level translators use VREF as the host-side voltage reference and the internal 1.8V digital IO core as the Wireless CPU®-side reference.

4.4   Grounds

Pin	Name	Direction	Function
2	GND	–	Ground
4	GND	–	Ground
6	GND	–	Ground
8	GND	–	Ground
10	GND	–	Ground
12	GND	–	Ground
60	AREF	–	Analogue reference

There are two ground connections in the Wireless CPU®, AREF (analogue ground) and GND (digital ground). Pin assignments are shown in the table above.

NOTE

AREF and GND are connected at a single point inside the Wireless CPU®; however they must not be joined together in the user application.

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4.4.1 Analogue Ground (AREF)

AREF is the return signal, or analogue audio reference, for AUXI and AUXO. These two signals provide a single-ended auxiliary audio input (host to Wireless CPU®) and output (Wireless CPU® to host). AREF is connected to the common GND inside the Wireless CPU® only. The application must not connect GND and AREF. AREF is to be used as a reference signal for the application AUXI and AUXO amplifiers (see figure below).
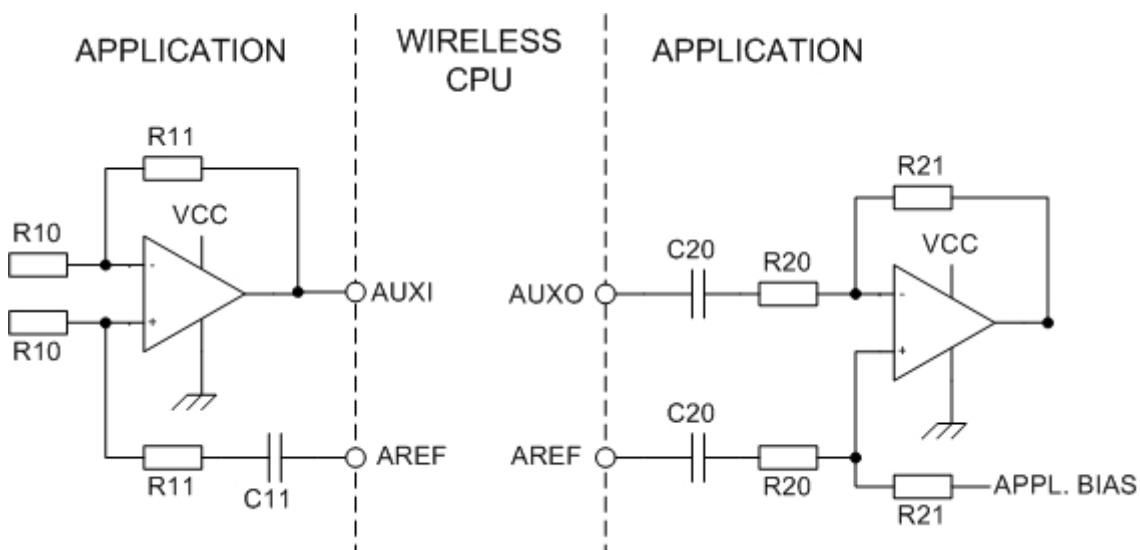
Figure 10: AREF implementation example for AUXI and AUXO

Parameter	Limit	Unit
Maximum current (I_{MAX})	12.5	mA

4.4.2 Common Ground (GND)

GND is the reference, or return signal, for all system interface digital signals, radio section power, and is also the DC return for the power supply, VCC.

To carry the high current drawn by the Wireless CPU®, the user application circuitry should connect all GND pins together.

Parameter	Per Pin	Total	Unit
Maximum current (I_{MAX})	600	3600	mA
Maximum average current (I_{AVG})	100	600	mA

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4.5　Regulated Power Supply Input (VCC)

Pin	Name	Direction	Function
1	VCC	Input	DC power
3	VCC	Input	DC power
5	VCC	Input	DC power
7	VCC	Input	DC power
9	VCC	Input	DC power

Power is supplied to the Wireless CPU® VCC pins, from an external source.

User application circuitry should connect all VCC pins together in to carry the current drawn by the Wireless CPU®.

The electrical characteristics for VCC are shown in the following table.

Parameter	Mode	Limit
VCC Supply voltage	Nominal	3.6 V
	Min	3.2 V
	Max	4.5 V
	Absolute maximum voltage range	–0.3V to 6.5V
	Maximum supply ripple	<100mV @<200kHz <20mV @>200kHz
Maximum allowable voltage drop	Transmission burst	200mV
Maximum current consumed	Full power (2W) transmit (single uplink slot)	2050 mA peak 330mA average

![WARNING] **Stresses in excess of the absolute maximum limits can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.**

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CAUTION

The Wireless CPU® has approximately 40μF of internal capacitance across the VCC pins. During initial power–up the host power supply will have to charge this capacitance to the operating voltage. This initial in–rush current may exceed the Wireless CPU®'s normal peak current, sometimes greater than an order of magnitude higher (depending upon the power supply design) for a short duration (generally a few microseconds).

TIP

The Wireless CPU® has insufficient internal capacitance to supply the large current peaks during GSM burst transmission – use the following general guidelines in designing the application power supply.

Fit a low ESR electrolytic capacitor close to the Wireless CPU® (>1,000 μF, with an ESR < 100 mohm)

Ensure power supply to Wireless CPU® line resistance is < 80 mohm

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4.6 Voltage Reference (VREF)

Pin	Name	Direction	Function
34	VREF	Input (Output)	Core voltage reference

GR64 provides a voltage reference interface for user applications.

Level translators are integrated in the GR64 product. The integrated level translators are referenced to an internal IO regulator on the Wireless CPU® side and to an application voltage on the user side of the interface (VREF). There are two implementations of VREF, dependent upon the users' GR64 variant;

- VREF as an output (GR64001 variants)
- VREF as an input (GR64002 variants)
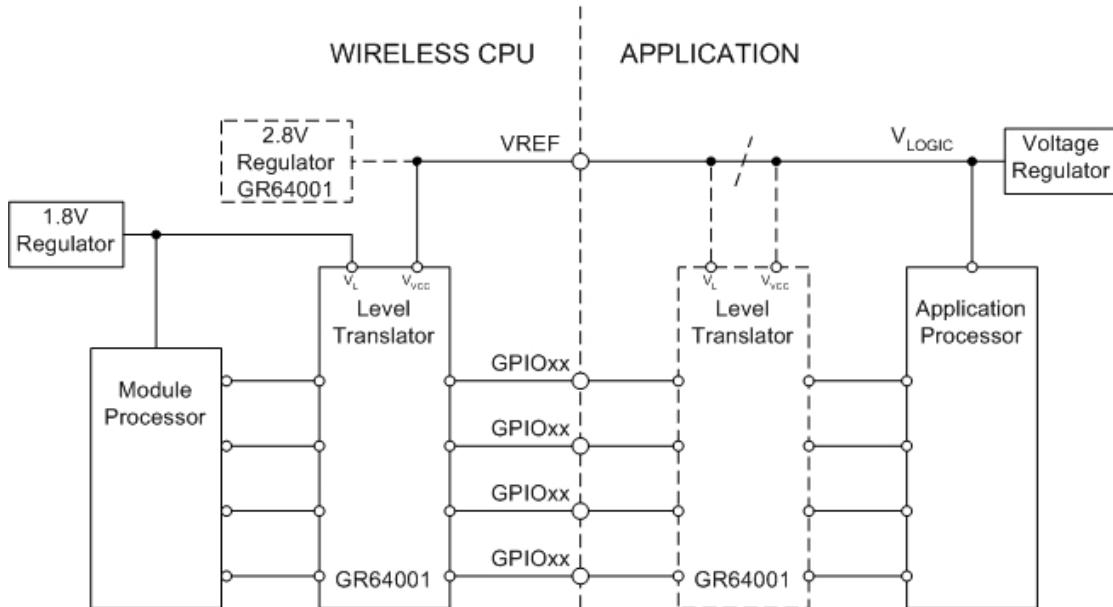
Figure 11: Level translator arrangement

The logic interface implementation will differ depending on the Wireless CPU® variant used. The table below describes how to design the interface depending on what Wireless CPU® is used.

Table 5: Interface implementation description

GR64 variant	Application Logic Voltage Level (V_{LOGIC})	Implementation Requirements
001	$2.6 > V_{LOGIC} > 3.0$	The application must implement level translators to re-reference its logic level to the logic level used by the Wireless CPU® interface.
	$2.6 < V_{LOGIC} < 3.0$	Connect the application logic signals directly to the GR64001 Wireless CPU® interface.
002	$1.8 \leq V_{LOGIC} \leq 5.0$	Connect the application logic supply voltage V_{LOGIC} to VREF of the GR64002 Wireless CPU®, and connect the application logic signals directly to the Wireless CPU® interface.

4.6.1 VREF as an Output from the Wireless CPU®

The GR64001 variants provide a 2.8V VREF reference output to the host side level translator devices. This enables legacy users, and users of older interface technology to connect directly to the GR64's IO. In this arrangement VREF can be used as a further level translator reference in the users application circuits, or to power external circuits, since it has a 75mA current sourcing capability.

Parameter	Min	Nom	Max	Unit
VREF output voltage	2.74	2.8	2.86	V
VREF load current			75	mA

⚠️ **WARNING** Note that at power down, this VREF pin will go high impedance. To ensure a low level after power down, implement a pull-down resistor. The value of the resistor depends on the application implementation.

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4.6.2   VREF as an Input to the Wireless CPU®

The GR64002 variants provide VREF as a reference input for the host side logic. This enables users of varying technologies to connect directly to the GR64's IO by providing a reference voltage from their own application IO. The application must apply their logic reference voltage on VREF and then connect their logic I/O's directly to GR64. This eliminates the need for level translators in the application.

Parameter	Min	Typ	Max	Unit
VREF input voltage	1.65		5.5	V
VREF load current		100	500	µA

4.7   Battery Charging Input (CHG_IN)

Pin	Name	Direction	Function
11	CHG_IN	Input	Battery charger power

For battery powered applications, the GR64 provides a charge input (CHG_IN) pin to aid and support battery charging. A typical application would power the Wireless CPU® directly from a battery source connected to VCC (pins 1, 3, 5, 7, 9) then provide a dc power source (CPS) to the CHG_IN connection (pin 11). The GR64 can control an internal switching FET which creates a charging pathway to the battery. While power is provided at CHG_IN, the battery charge can be maintained. If the power should fail or be removed at CHG_IN, the application will be supported by the battery alone. When CHG_IN voltage returns, the battery charging and maintenance will commence once more.

Parameter	Min	Typ	Max	Unit
CHG_IN input voltage	4.5	5.5	6.0	V
CHG_IN current			500	mA

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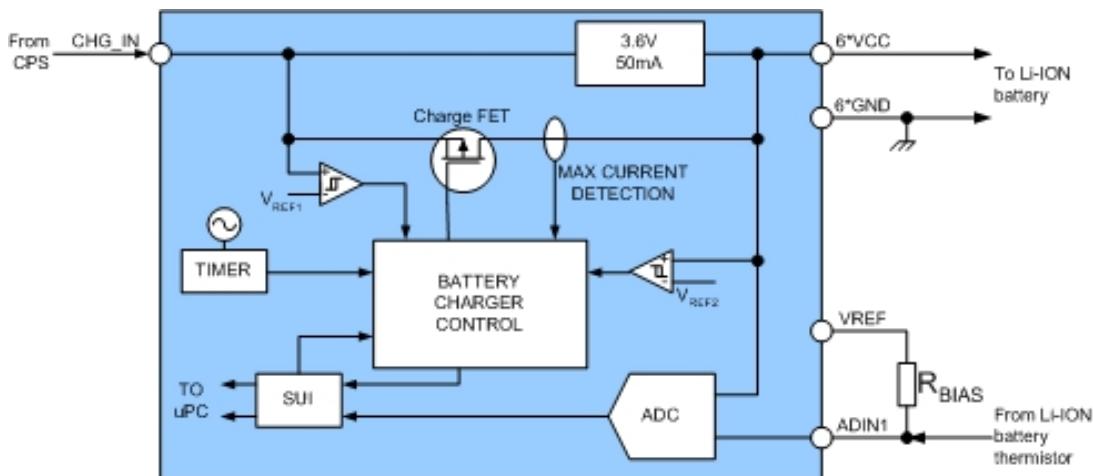
Figure 12: GR64 Charger Implementation

The GR64 Wireless CPU® supports only one mode of charging, microprocessor supervised pulsed-charging. Also, the Wireless CPU® only supports one battery cell type as standard.

DANGER	Battery charging algorithms are unique to different battery types. Wavecom will not accept any responsibility or liability for damage, product failures, even death or injury occurring as a result of incompatible battery and charging algorithms being applied.

Safety considerations must be taken into account when using the battery charge function of the GR64; for example, monitoring the temperature of the battery. If the temperature of the battery exceeds its specification limits, battery charging must be stopped immediately. If the battery temperature continues to rise the application should be suspended or the battery disconnected. Battery temperature can be monitored with a suitable detection circuit, using the GR64 ADC1 input.

CAUTION	When charging Lithium batteries, the battery pack must have an internal protection circuit in accordance with the battery manufacturer's instructions.

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During microprocessor supervised mode, the GR64 takes a current–limited voltage source at the CHG_IN pin to implement constant–current charging of a single Li–Ion cell connected to the VCC pins.
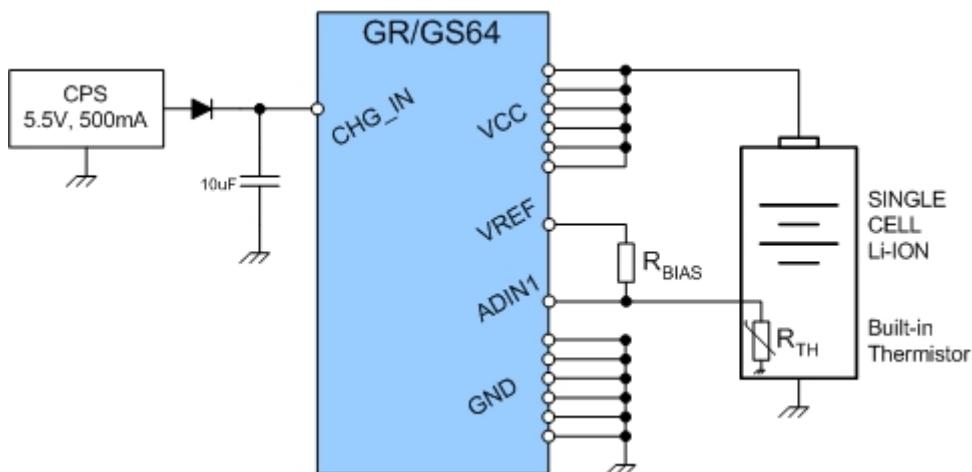
Figure 13: Typical application for pulse charging a battery

4.7.1   Charging Process

Figure 13 shows a typical battery charging implementation. The voltage source must be current limited (500 mA max). A reverse current protection diode prevents external fault conditions from draining the battery. A small (typ 10µF) capacitor should be placed close to the CHG_IN pin.

In the application shown, a conditioning phase slowly raises the voltage of a deeply discharged battery cell to a level suitable for fast–charging. After cell conditioning is complete, the microprocessor uses the GR64'S ADC converter to monitor the cell's status and uses the power management block to control the charge–FET.

A charge request is initiated when an external voltage source (CPS) is applied to the CHG_IN pin. However, before this request is passed to the microprocessor, CHG_IN is verified to be greater than VCC by 150 mV, and at least 3.7 V. If the latter criterion is not met, the Wireless CPU® limits charging to the conditioning phase. If the former criterion is not met, the charge request is ignored and all charging is disabled. If the CHG_IN voltage exceeds the upper limit of 6.3 V it will be detected by the Wireless CPU®, but charging is not inhibited. In this case, however, CHG_IN is outside the normal operating range of the device, so the software will not initiate charging if CHG_IN > 6.3 V is detected.

The delta between CHG_IN and VCC is continuously monitored; however, the valid to invalid detection has a delay of 46 ms. When CHG_IN exceeds VCC by 150 mV, it is considered to be at a valid relative level. It is considered to have an invalid relative

level if it subsequently falls below VCC by 50 mV. If the relative voltage of CHG_IN goes invalid and remains invalid for the duration of the detection delay, charging is terminated.

As a safety precaution, the battery cell voltage must be at least 2.5 V before fast-charge is allowed to take place. If the battery cell voltage is less than 2.5 V, it is considered either deeply discharged or shorted. To protect a Li-ion cell from the damage that may occur if it is fast-charged from this state, a 3.6 V trickle-charge source is used to safely condition the battery cell. The conditioning charge current is limited to 50 mA, which for most Li-ion cells is 10% or less of the recommended CC fast-charge current. In most instances, the battery cell voltage will be greater than 2.5 V at the time the charge request is initiated, resulting in the conditioning phase being skipped.

CAUTION	There is always a small chance that the charge management block in the GR64 power management ASIC will malfunction or fail, which could lead to over-charging of the battery. It is strongly recommended that any battery chosen for use with the application has its own additional integrated over-current and over-voltage protection.

4.7.2   Series Diode

When charging is disabled, the potential for rapid cell discharge through the body diode inherent in the Enhancement-mode charging FET, a Schottky diode must be placed in between the external source and the CHG_IN pin. The diode should have a forward current and power dissipation rating consistent with its intended use, and a maximum forward voltage drop of 0.6V.

4.7.3   Battery Selection

Whilst there are several rechargeable battery technologies commercially available, including Nickel Cadmium (NiCd), Nickel Metal Hydride (Ni-MH), Lithium-Polymer (Li-Polymer) and Lithium-Ion (Li-Ion), the only technology recommended and supported for use with the GR64 is Li-Ion. Li-Ion provides a good combination of high energy (3.7V) and long cycle life, which lead to low overall energy cost.

The weight of lithium ion batteries is approximately one half compared with a nickel cadmium or nickel metal hydride battery of similar capacity. The volume of lithium ion batteries is 40-50% smaller than that of nickel cadmium and 20-30% smaller than that of a nickel metal hydride.

The lithium ion battery is free from the so-called memory effect, a phenomenon associated with nickel cadmium in which the apparent battery capacity decreases when shallow charge and discharge cycles are repeated.

A single lithium ion cell has a voltage of 3.7V (mean value), which is equal to either three nickel cadmium or nickel-metal hydride cells connected in series. This voltage is close to the nominal VCC of the GR64 device.

Li-Ion batteries generally provide long storage life with few limiting condition, and offer problem-free charge after long storage. Under normal conditions, the lithium ion battery has a life of more than 500 charge/discharge cycles. Also, Li-Ion batteries have a slow self-discharge rate (typically 1.3% per month, compared with Ni-MH batteries which can exceed 50% per month).

Lithium ion batteries are environmentally friendly, inasmuch as they do not contain any heavy metal pollution substances such as cadmium, lead, or mercury.

There are many manufacturers of Li-Ion batteries worldwide. Wavecom makes no recommendations with regard to specific vendors, but here are some considerations for GR64 users which may prove to be useful in the selection process and implementation:

- Li-Ion batteries marketed for cellular (mobile) phone use may make a good choice

- battery manufacturers with heritage in supplying the cellular (mobile) phone industry could make a good choice, especially for high-volume requirements

- look carefully for batteries which are rated at temperatures that the GR64 is likely to operate at (many batteries are only specified for −20°C to +65°C operation which may not be sufficient)

- small form-factor (typically handset-sized) Li-Ion battery capacity varies considerably, some batteries are rated as high as 3200mAh (600mAh to 1800mAH are more commonly available)

- weight is generally not a problem with typical GR64 user application, even so small form-factor Li-Ion batteries (up to 1800mAh) can vary between 10 to 40 grams

- size is generally a factor of capacity, since larger capacity batteries naturally have more material/cells, and will range between 2750mm3 to 18000mm3 for small form-factor Li-Ion batteries

- the speed by which lithium-ion ages is governed by temperature and state-of-charge; high temperatures and deep discharge will effect useful life

- if possible avoid frequent full discharges because this puts additional strain on the battery, partial discharges with frequent recharges are better

- never short circuit the terminals of a Li-Ion battery

- do not expose Li-Ion batteries to moisture or rain

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- monitor battery temperature during charging using a thermistor placed on or near the battery wired to an ADC input on the Wireless CPU®

Li-Ion batteries have a higher ESR (compared to Ni-Cd or Ni-MH), although this should not be a limiting factor for peak current delivery, any battery should be capable of at least 50% greater than the GR64 demands (~3A peak)

To determine battery life, on a full charge, the following rule of thumb can be applied:

- Standby time = Battery Capacity (mAh) / Idle current (mA)
- Call time (voice or data) = Battery Capacity (mAh) / Call current (mA)

Example 1 – Standby Time

A 600mAh rated Li-Ion battery, from fully charged (around 4.2V) to the Wireless CPU® cut-off point (3.2V) will provide around 95% of its total charge capacity. For a standby (idle) current of 18mA, the Wireless CPU® will typically provide

600*0.95/18 = 32 hours standby time

Example 2 – Call Time

An 1800mAh rated Li-Ion battery fully charged, transmitting maximum power on a low-band (850/900MHz) channel may consume an average 320mA, therefore the Wireless CPU® would typically provide

1800*0.95/320 = 5 hours 20 mins call time

Example 3 – Typical Operation

A Wireless CPU® performing periodic network data transfers and communicating intervallic status information to its host would spend its non-active periods in sleep mode. If the Wireless CPU® spends 30 minutes each day on call (320mA), 30 second each hour performing housekeeping, monitoring and status tasks (110mA), and sleeps (2.1mA) during the intervening periods, an 1800mAh rated Li-Ion battery fully charged would typically provide

1800*0.95/([0.5hr*320]+[0.2hr*110]+[23.3hr*2.1]) = 7 days 6 hrs operation

CAUTION

The above examples are given for guidance, the actual battery life will depend upon variables such as battery condition, number of previous charge/discharge cycles, operating temperature, series resistance between battery and the Wireless CPU®, and manufacturing tolerances

4.8 Powering the Wireless CPU® ON and OFF (ON/OFF)

Pin	Name	Direction	Function
14	ON/OFF	Input	Device on/off control

The ON/OFF description below references a GR64001 Wireless CPU® variant. The timing is also valid for the GR64002 variant with the exception that VREF can be excluded since it is input to the Wireless CPU® by the application. VREF shall in the GR64002 variant implementation be seen as the Wireless CPU®'s internal logical voltage supply.

4.8.1 Turning the Wireless CPU® On
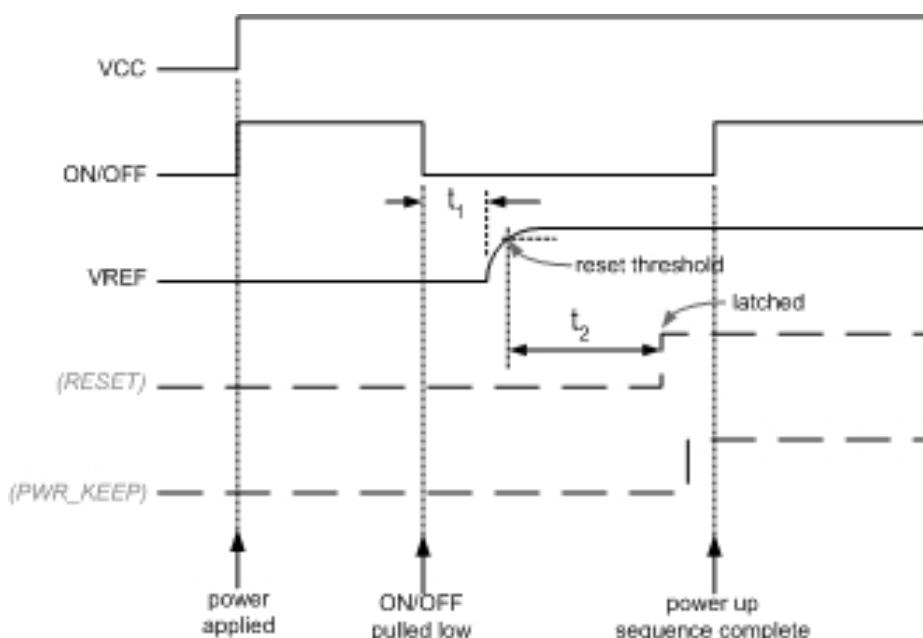
Figure 14: Power On timing for GR64001

The GR64 power ON sequence is shown above. The significant signals are VCC, ON/OFF and VREF, shown by solid lines. The other signals (in dashed lines) are internal to the Wireless CPU® and are shown for reference purposes only.

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Initially, power is supplied to the VCC pins. The presence of power raises the ON/OFF through a pull-up resistor to VCC potential. In order to power the Wireless CPU®, ON/OFF is pulled to ground. Once ON/OFF has been held low for 125ms (denoted by t1) the primary LDOs power up; the VREF signal comes from one of the primary LDOs. For Wireless CPU® variants where VREF supplies a reference voltage to the host, it acts as a useful indicator that the Baseband is powered.

NOTE When the VREF is configured as an input, it cannot be used as a power indicator.

VREF exceeds its reset threshold approx 500μs later, and then 250ms afterwards (denoted by t2) the RESET line goes high. The microprocessor can latch the power on state by setting the power keep (PWR_KEEP) high after the RESET goes high and before the power on (ON/OFF) signal is released.

It is recommended that ON/OFF is held low for at least 450ms to guarantee completion of the power up sequence.

4.8.2   Turning the Wireless CPU® Off
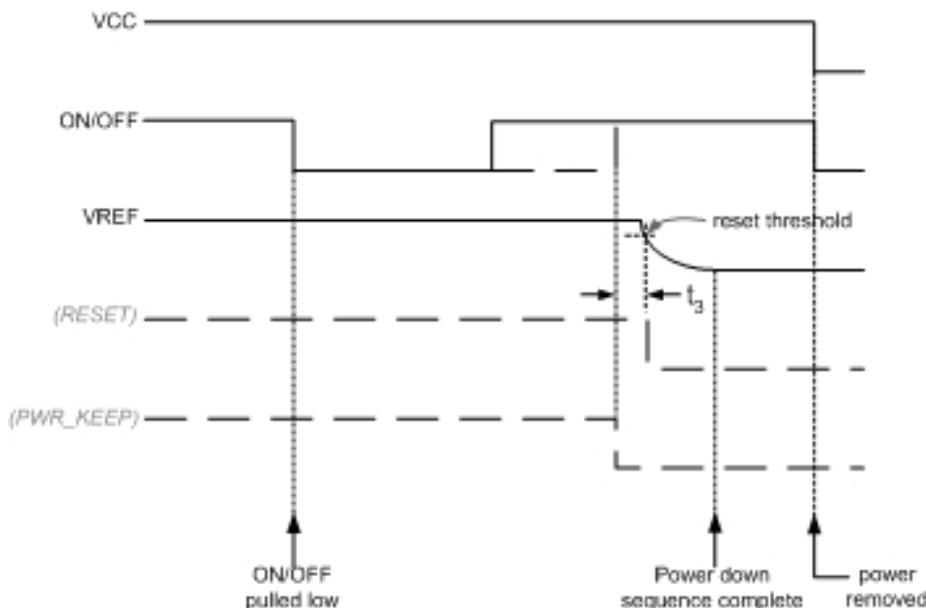
Figure 15: Power Off timing for GR64001

| ![WARNING] | Failure to implement the proper shut down procedure could result in permanent damage to the device including, but not limited to, erasure of critical parameters stored in non-volatile memory. Product warranty is invalidated in such circumstances. |

Powering the GR64 power down sequence is shown above. The significant signals are VCC, ON/OFF and VREF, shown by solid lines. The other signals (in dashed lines) are internal to the Wireless CPU® and are shown for reference purposes only.

With the Wireless CPU® powered normally, ON/OFF is pulled–up to VCC potential. In order to power down the Wireless CPU®, ON/OFF is pulled to ground. Once ON/OFF has been held low for at least 125ms the shut-down procedure begins. Although ON/OFF can be held low for longer time, it will only delay completion of the shut–down event. If the Wireless CPU® is registered on a GSM network, the de–registration process will complete; this may last between 3 to 30 seconds. The power latch (PWR_KEEP) is released and approximately 70ms later the LDO outputs fall, unless ON/OFF is held in which case the LDO's will be kept active until ON/OFF is released.

For Wireless CPU® variants where VREF is an output, the absence of VREF is a useful indicator that the networks de–registration and shut–down is complete. Once VREF is no longer present, the application can safely remove VCC.

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The RTC can continue to operate even though VCC is removed, provided that a sufficiently charged backup device is connected to the VRTC. Refer to section 4.20 for details.

The relevant characteristics of the ON/OFF Power control interface are shown in the table below.

Parameter	Conditions	Min	Typ	Max	Unit
Input current	Input low (0V), VCC = 3.6V	−60	−25	−12	μA
	Input high (VCC), VCC = 3.6V	0		1	μA

4.9 Analogue Audio

	Pin	Name	Direction	Function
Low–level	53	MICIP	Input	Microphone input positive
Low–level	54	MICIN	Input	Microphone input negative
Low–level	55	EARP	Output	Earpiece output positive
Low–level	56	EARN	Output	Earpiece output negative
High–level	57	AUXO	Output	Auxiliary audio from Wireless CPU® to host
High–level	59	AUXI	Input	Auxiliary audio to Wireless CPU® from host
High–level	60	AREF	–	Analogue reference

The analogue audio signals comprise of two audio inputs to the Wireless CPU®, and two audio outputs from the Wireless CPU®. The Auxiliary interface signals are single-ended, whilst the MIC and EAR interface signals are differential. Analogue audio can be used for various configurations, including handset, car kit, portable hands free and speakerphone mode (with an additional output gain stage).

Five audio profiles are available for GR64 users to configure various modes of operation. Each profile is factory set to represent different modes, typical of general usage. The customer can modify profiles to optimize acoustic performance to their specific application.

The analogue inputs and outputs share common uplink and downlink chains which are multiplexed, and selectively switched by the user through AT-commands.

4.9.1   Auxiliary Audio to Wireless CPU® (AUXI)

AUXI is a single-ended auxiliary analogue audio input to the Wireless CPU®. Internally, the signal is routed to the CODEC (Coder/DECoder), where it is converted to digital audio and mapped to an internal bus.
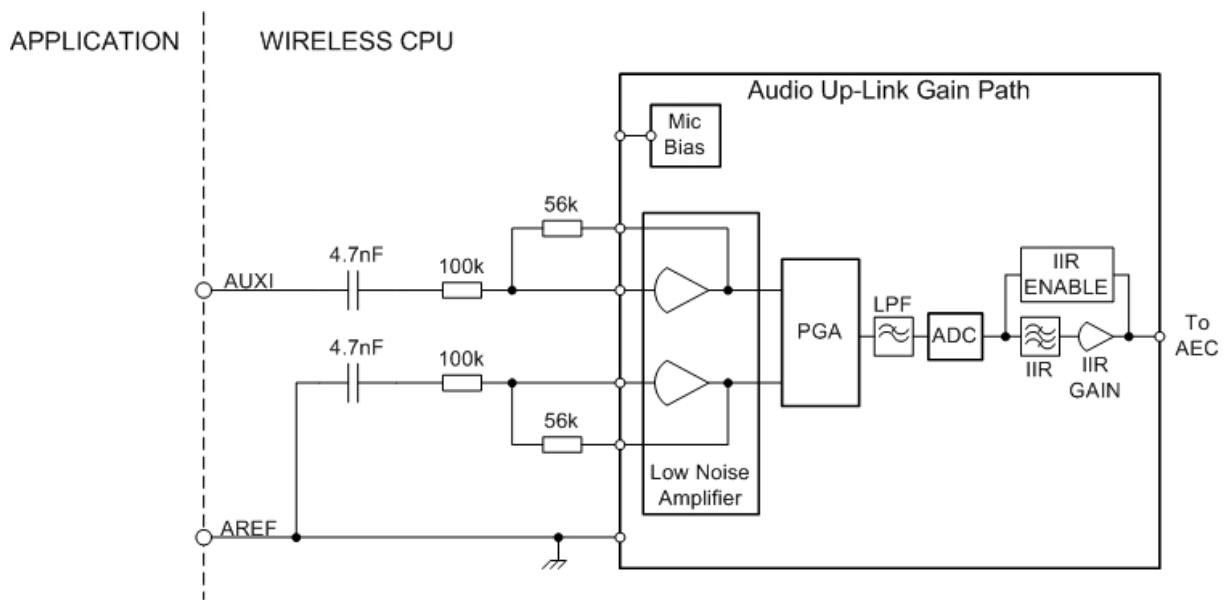
Figure 16: Auxiliary input connections to the Wireless CPU®

The AUXI input is a passive network applying -5dB of gain followed by the transmit part of the CODEC.

Parameter	Conditions	Min	Typ	Max	Unit
Input voltage full scale	max input gain	142	158	178	mVrms
	min input gain	447	501	564	mVrms
Frequency response	-3dB cut-off	340		3400	Hz
AC input impedance	300-3400 Hz		100		kohm

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4.9.2   Auxiliary Audio from Wireless CPU® (AUXO)

AUXO is a single-ended auxiliary analogue audio output from the Wireless CPU® and may be used to drive a speaker or an earpiece. The interface has an internal 100nF coupling capacitor; a load of 10kohm will provide a near full-scale output capability between 300 to 4300 Hz.
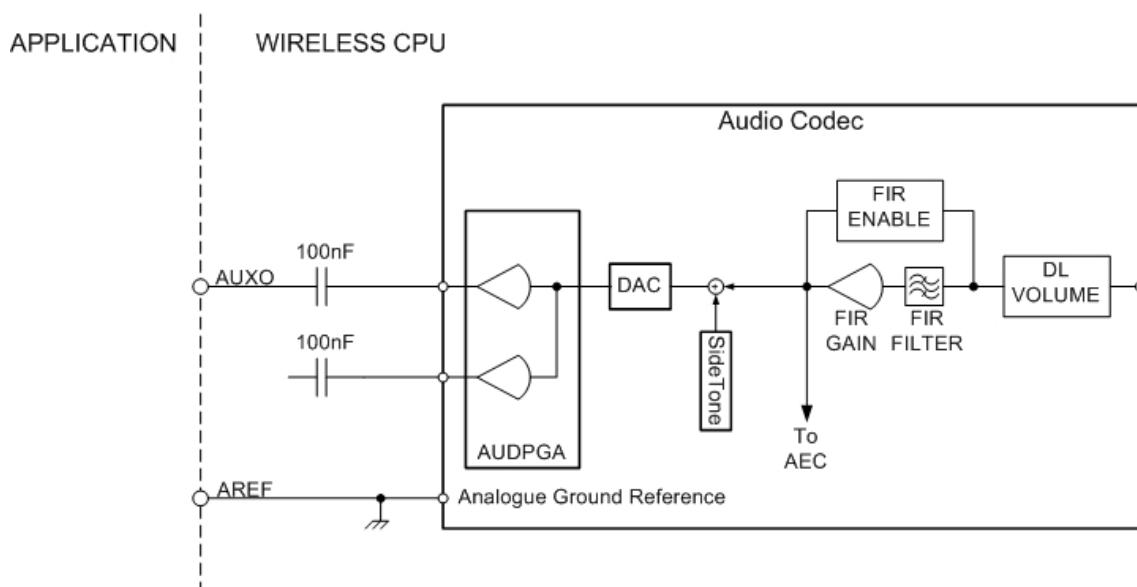
Figure 17: Auxiliary output connections to the Wireless CPU®

The table below shows the audio signal levels for AUXO.

Parameter	Conditions	Min	Typ	Max	Unit
Output voltage full scale	RL =10kΩ	670	750	840	mVrms
Frequency response HPF	−3dB cut-off (RL =10kΩ)		160		Hz

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4.9.3   Microphone Signals (MICIP, MICIN)

MICIP and MICIN are balanced differential microphone input pins. These inputs are compatible with an electret microphone. The microphone contains a FET buffer with an open drain output, which is supplied with at 2.4V ±10% relative to ground by the Wireless CPU® as shown below.
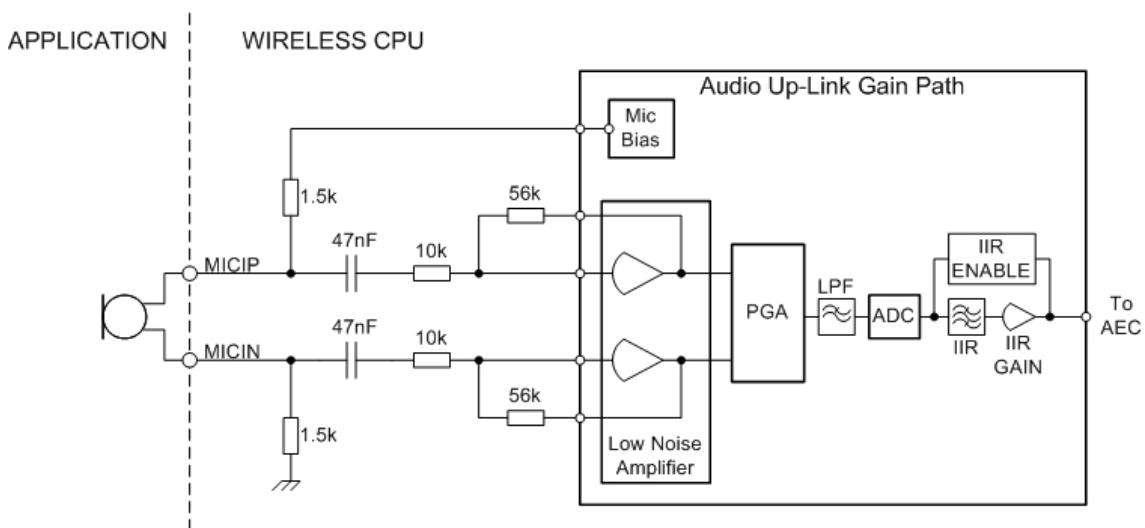
Figure 18: Microphone input connections to the Wireless CPU®

The input low-noise amplifier stage is constructed out of standard low-noise op amps. External resistors set the gain of this stage.

The input gain is scaled by the input resistors to be around 15dB, which provides optimal performance for many standard types of electret-microphones. An additional gain adjustment can be made through an AT-command to the PGA which can be set to high and low gain. The Wireless CPU® provides a microphone bias at 2.4V, and can supply at least 1mA of current.

Parameter	Conditions	Min	Typ	Max	Unit
Input voltage full scale	max input gain	14	16	18	mVrms
	min input gain	45	50	56	mVrms
Frequency response	–3dB cut-off	340		3400	Hz
AC input impedance	300–3400 Hz		10		kohm
Output dc bias level		2.16	2.4	2.64	V

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4.9.4 Speaker Signals (EARP, EARN)

EARP and EARN are the speaker output signals. These are differential–mode outputs. With a full–scale PCM input to the CODEC, 0 dB audio output gain setting, and a differential load RL = 30 ohm, the output voltage between EARP and EARN is 1.5 V rms. For load resistances less than 30 ohm, the full–scale output needs is limited using the Wireless CPU®'s internal programmable gain attenuator.
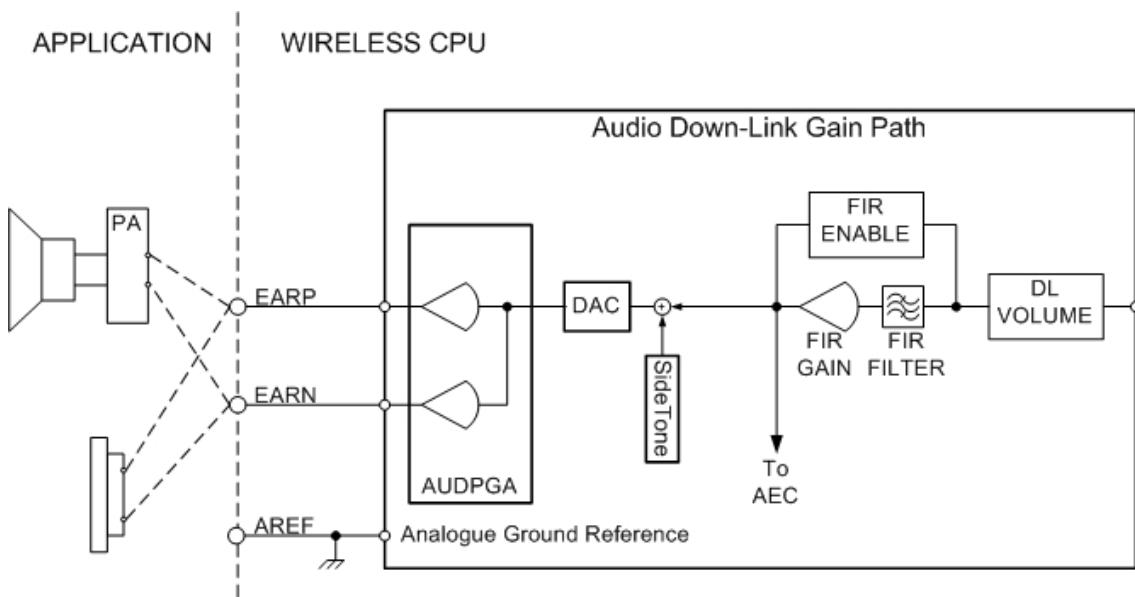
Figure 19: EAR output connections to the Wireless CPU®

The electrical characteristics are given in the table below.

Parameter	Conditions	Min	Typ	Max	Unit
Output voltage full scale	RL = 30 ohm	1.34	1.5	1.68	Vrms
	RL = 16 ohm	1.41			Vrms
	RL = 8 ohm	1.24			Vrms
Frequency response	–3dB cut–off	300		3400	Hz

4.10 PCM Digital Audio (SSP)

Pin	Name	Direction	Function
48	SSPDFM	Output	Serial PCM data from Wireless CPU® to host
47	SSPDTM	Input	Serial PCM data to Wireless CPU® from host
51	SSPFS	In/Out	Serial PCM frame synchronisation
52	SSPCLK	In/Out	Serial PCM clock

The SSP (Synchronous Serial Port) digital interface is configured to provide a PCM (digital) audio interface. This interface can be used to process PCM digital audio signals as an alternative to routing signals to the CODECs through the analogue uplink and downlink chains.
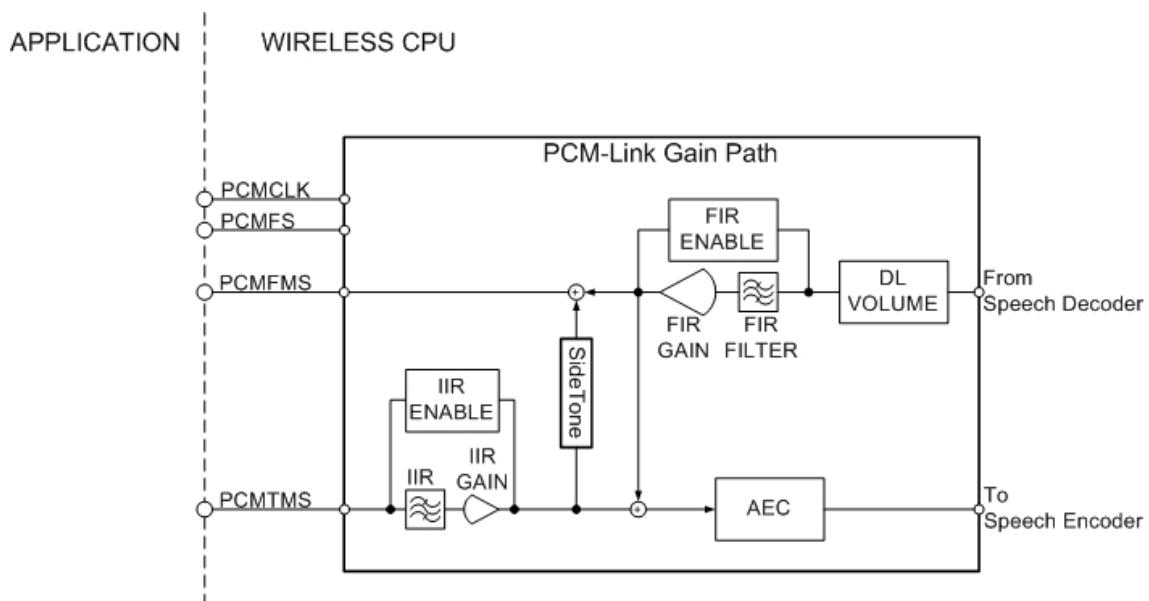
Figure 20: PCM audio path

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4.10.1 PCM Data Format

The PCM digital audio interface for GR64 is based upon the Texas Instruments SSI standard. The SSP interface can be programmed for data frame sizes between 4 to 16 bits. The clock rate is fixed to 128kHz.

PCMCLK (bit clock) and PCMSYNC (frame synchronization) are both generated by the DSP within the Wireless CPU®. The DSP within the Wireless CPU® in this instance is the master for all external PCM, so clocks and data from external devices must be synchronized to it.

For standard GSM voice a 13-Bit PCM data word is embedded in a 16-bit word frame, as shown in Figure 21 below.

Figure 21: 13-bit GSM voice embedded in 16-bit PCM Frame

Typical PCM data transfer is shown in the following figures.
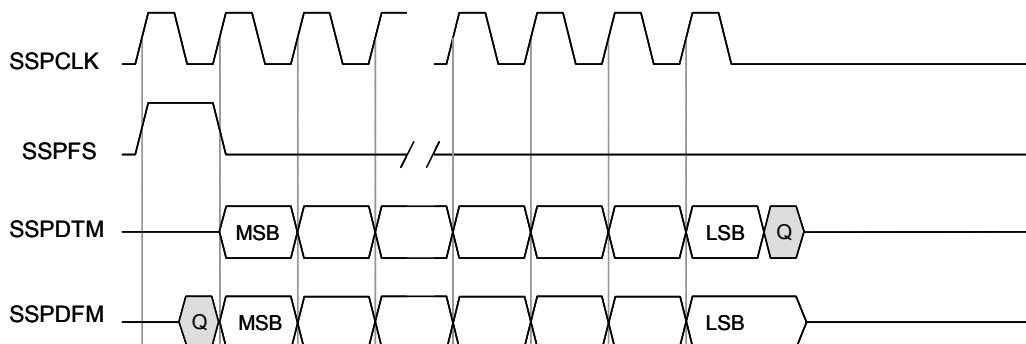
Figure 22: PCM Frame format for a single transfer

Q in Figure 22 above indicates unknown or invalid data content which should be disregarded.
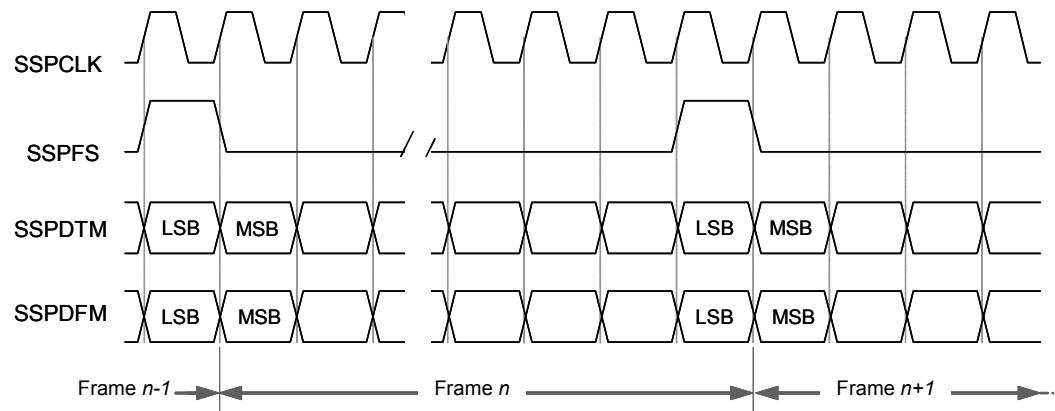
Figure 23: PCM Frame format for a continuous transfer

4.11 Serial Data Interfaces

The serial channels consist of two UARTs and a USB port. These provide communication links to the application or accessory units.

The serial channels can be used in differing configurations, depending upon the user's requirements and application. However, the common configuration options are described:

- UART1 has full RS-232 functionality and is used for all on- and off -line communication (modem sleep & wake functional control is an integral component of this interface). Its intended use is that of the primary command (AT) interface.

- UART3 behaves as a general-purpose serial data link. It can be used for data logging and de-bugging purposes. A GPS device can be used with UART3 as part of an embedded application.

- The USB port, available on the GR64002 variants, provides a convenient general purpose peripheral (slave) port for use with host devices which have USB controllers.

4.11.1 UART1

Pin	Name	Direction	Function
32	DSR1	Output	Data Set Ready (UART1)
36	RI	Output	Ring Indicator
37	DTR1	Input	Data Terminal Ready (UART1)
38	DCD1	Output	Data Carrier Detect (UART1)
39	RTS1	Input	Ready To Send (UART1)
40	CTS1	Output	Clear To Send (UART1)
41	DTM1	Input	Data To Wireless CPU® from host (UART1)
42	DFM1	Output	Data From Wireless CPU® to host (UART1)

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UART1 is a full featured Universal Asynchronous Receiver Transmitter providing full-duplex asynchronous communication.

UART1 has the following features:

- 32 bytes of FIFO for both receive and transmit
- FIFO threshold interrupts
- 1 start bit, 7 or 8 data bits, 1 optional parity bit, 1 or 2 stop bits
- Programmable baud rate
- Auto-configuration mode with auto-baud and auto-format operation
- Hardware flow control
- Software flow control.

Depending upon the user application, some, all, or none of the control signals may be needed.   Each of the control signals can alternatively be configured as a general purpose IO. When hardware flow control is not used in communications between the application and the Wireless CPU®, some applications may require RTS and CTS to be connected to each other at the Wireless CPU®. Users should familiarize themselves with the specific implementation of their UART.

The GR64 has a feature in which sleep (lower power) mode can be controlled through a special handshake protocol using hardware flow control. Details of this protocol and the AT commands associated with it are contained in a special Application Note, obtainable through the normal customer support channel.

UART1 converted signals, together with GND, DTM1 and DFM1 form a 9-pin RS232 data port.

The electrical characteristic of this level-shifted signal is described in section 4.3.1.1.

UART1 signals replicate a 9-pin RS232 (V.24) serial port. However, UART1 signal levels are not compliant with the RS232 (V.28) standard. Conversion between the Wireless CPU® CMOS levels and RS232 levels can be achieved using a standard interface IC, such as the Maxim Integrated Products MAX3237. The relationship between the levels is shown in the following table:

DTM, DFM	RI,RTS,CTS,DSR,DTM,DCD	RS232 level	GR64 level
1	OFF	<-3V	VREF
0	ON	>+3V	0 V

4.11.1.1 Serial Data Signals (DTM1, DFM1)

The default baud rate of the UARTs is auto-baud. Baud rates of between 600 bauds to 460k bauds are possible. The Wireless CPU® also supports 3GPP TS 27.010 multiplexing protocol, which starts when the appropriate command is sent.

4.11.1.1.1 Serial Data From Wireless CPU® (DFM1)

DFM1 is an output signal that the Wireless CPU® uses to send data via UART1 to the host application.

4.11.1.1.2 Serial Data To Wireless CPU® (DTM1)

DTM1 is an input signal, used by the application to send data via UART1 to the Wireless CPU®.

4.11.1.2 Control Signals (RTS1, CTS1)

RTS and CTS provide a hardware flow control mechanism.

4.11.1.2.1 Request to Send (RTS1)

RTS is used to condition the DCE for data transmission. The default level is high by internal pull up. The application must pull RTS low to enable data transmission from the Wireless CPU®. Similarly, the Wireless CPU® asserts CTS low, indicating it is ready to receive data transmission from the host.

4.11.1.2.2 Clear To Send (CTS1)

CTS is asserted by the DCE to indicate that the host (DTE) may transmit data. When CTS is high, the host (DTE) is not permitted to transmit data. The table below shows the load characteristics for this signal.

4.11.1.3 Control Signals (DTR1, DSR1, DCD1, RI)

4.11.1.3.1 Data Terminal Ready (DTR1)

DTR indicates that the DTE is ready to receive data. It also acts as hardware 'hang-up', terminating calls when switched high. The signal is active low. Users can define the exact behaviour of DTR with the AT&D command. DTR1 is used as an optional sleep control mechanism when the Wireless CPU® is configured appropriately.

4.11.1.3.2 Data Set Ready (DSR1)

DSR indicates that the DCE is ready to receive data. The signal is active low. Behaviour is controlled using the AT&S command. DSR1 is used as an optional sleep control mechanism when the Wireless CPU® is configured appropriately.

4.11.1.3.3 Data Carrier Detect (DCD1)

DCD indicates that the DCE is receiving a valid carrier (data signal) when low. Behaviour is controlled using the AT&C command.

4.11.1.3.4 Ring Indicator (RI)

RI indicates that a ringing signal is being received by the DCE when toggled low. Users can define the exact behaviour of RI with an AT command, including the option of asserting the RI signal to flag an incoming SMS by using the AT*E2SMSRI command.

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4.11.2 UART3 (DTM3, DFM3)

The reason UART2 is skipped is that GR64 does not support more than two UART interfaces. The removed interface was represented by UART2 for the GR47/48, so for legacy reasons the second UART in GR64 is called UART3.

Pin	Name	Direction	Function
43	DTM3	Input	Data To Wireless CPU® from host (UART3)
44	DFM3	Output	Data From Wireless CPU® to host (UART3)

UART 3 consists of a full duplex serial communication port with transmission and reception lines.

Timing and electrical signals characteristics are the same as for UART1, DTM1 and DFM1, including the baud rate range and the capability to auto-baud.

TIP
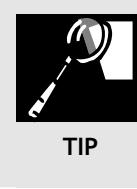
This interface is used by Wavecom for degug logging. It is strongly recommended that this interface is made available in case the application needs to be debugged.

4.11.2.1 Transmitted Data (DTM3)

DTM3 is used by the application to send data to the Wireless CPU® via UART3. It has the same electrical characteristics the equivalent signal in UART1.

4.11.2.2 Received Data (DFM3)

DFM3 is used to send data to the application via UART3. It has the same electrical characteristics as the equivalent signal in UART1.

4.11.3 USB

Pin	Name	Direction	Function
45	USBDP	In/Out	USB data positive
46	USBDN	In/Out	USB data negative
49	VUSB	Input	USB DC power

The USB interface is compliant with the USB2.0 standard for a full speed (12Mbps) endpoint device. Together with VUSB and GND it creates a standard USB 4-pin interface. VUSB (VBUS in the USB standard) is nominally 5.0V.

Parameter	Conditions	Limit			Unit
		Min	Typ	Max	
VUSB	Input voltage level	4.5	5.0	5.5	V
I_{VUSB}	Current consumption (VUSB=5.0V)		8	15	mA

NOTE	USB is not available on legacy variant GR64 devices (GR64001 products). On these products, the signal connections can be left un-terminated.

The USB interface has the following features:

- Full-speed (12M bits/s) device operation
- 16 unidirectional endpoints
- Each endpoint capable of supporting control, interrupt, isochronous and bulk transfer
- Programmable endpoint types and FIFO sizes and internal 1120-byte logical (2240-byte physical for dual-packet mode) shared FIFO storage allow a wide variety of configurations.
- Dual-packet mode of FIFOs reduces latency
- USB reset can be programmed to clear device address.

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- Firmware ability to wake up and reset a suspended device

- 8, 16, 32, and 64-byte FIFO sizes for non-isochronous transfers

- 64, 256, 512, and 1024-byte FIFO sizes for isochronous transfers

- Trace debug port for Wireless CPU® diagnostics

The USB interface supports 3GPP TS 27.010 multiplexing, and may be used as the primary AT-command interface.

Internally, the USBDP line is pulled up by a 1.5K resistor, in accordance with the USB standard, to indicate that it's a full-speed capable device to the USB controller.

To implement successful applications using the GR64 USB interface, users should familiarize themselves with the USB specification.

4.12 SIM Card Interface

Pin	Name	Direction	Function
15	SIMVCC	Output	1.8V or 3.0V SIM card supply
16	SIMDET	Input	SIM presence detection
17	SIMRST	Output	SIM card reset signal
18	SIMDAT	In/Out	SIM card data
19	SIMCLK	Output	SIM card clock signal

This interface allows the user to communicate with the smart (SIM) card in the user application. The GR64 offers alternative arrangements for accessing the SIM depending on which variant of the GR64 is used. Both variants provide this interface through the system connector, referred to as the external or remote SIM interface to distinguish it from the integrated SIM interface.

NOTE	The maximum distance between the SIM card holder and the Wireless CPU® varies depending on the application implementation. SIM holders placed too far away from the Wireless CPU® may not meet the SIM interface performance specification.

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This SIM interface allows the use of 3 V and 1.8 V SIM cards (5V is unsupported). The Wireless CPU® automatically detects the SIM type, switching the signal voltages accordingly.

Signal	Parameter	Mode	Min	Typ	Max	Unit
SIMVCC	SIM supply voltage	1.8	1.71	1.8	1.89	V
		3.0	2.75	2.9	3.05	V
	Short circuit current		10			mA
	Quiescent Supply Current	3.0		20		µA
	Output Capacitance		0.3		2.0	µF
	Output Capacitor ESR		0.01		1.0	ohm
SIMDAT	High level input voltage (VIH)	1.8			0.7*SIMVCC	V
		3.0			0.7*SIMVCC	V
	Low level input voltage (VIL)	1.8	0.2*SIMVCC			V
		3.0	0.4			V
	High level output voltage (VOH)	1.8	0.8*SIMVCC			V
		3.0	0.8*SIMVCC			V
	Low level output voltage (VOL)	1.8			0.4	V
		3.0			0.4	V
SIMCLK / SIMRST	High level output voltage (VOH)	1.8	0.9*SIMVCC			V
		3.0	0.9*SIMVCC			V
	Low level output voltage (VOL)	1.8			0.4	V
		3.0			0.4	V

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4.12.1 SIM Detection (SIMDET)

SIMDET is used to determine whether a SIM card has been inserted into or removed from the SIM card holder. The integrator should normally wire it to the 'card inserted switch' of the SIM card holder, but different implementations are possible.

An internal pull–up resistor keeps the SIMDET–signal at a high level (1.8V) when left open. This means 'SIM card missing' to the Wireless CPU®. When pulled low the radio device assumes a SIM card is inserted. SIMDET is a Digital IO signal input with characteristics defined in section 4.3.

NOTE	It is possible to use the external SIM even if SIMDET is not set low. If a SIM is inserted in the SIM–holder external to the Wireless CPU®, the application can send AT*ESSE=1 and the Wireless CPU® will switch to the external SIM regardless of the status of SIMDET.

4.13 Service/Programming

Pin	Name	Direction	Function
58	SERVICE	Input	Flash programming enable signal

The SERVICE interface is flash programming enable input. The SERVICE pin is driven active high by the host application using either a logic control input or applying a dc voltage (common in legacy applications) to begin a flash download. This pin should be pulled low or grounded during normal use.

The SERVICE signal drives an N-channel FET switch which has a resistive divider on the input.
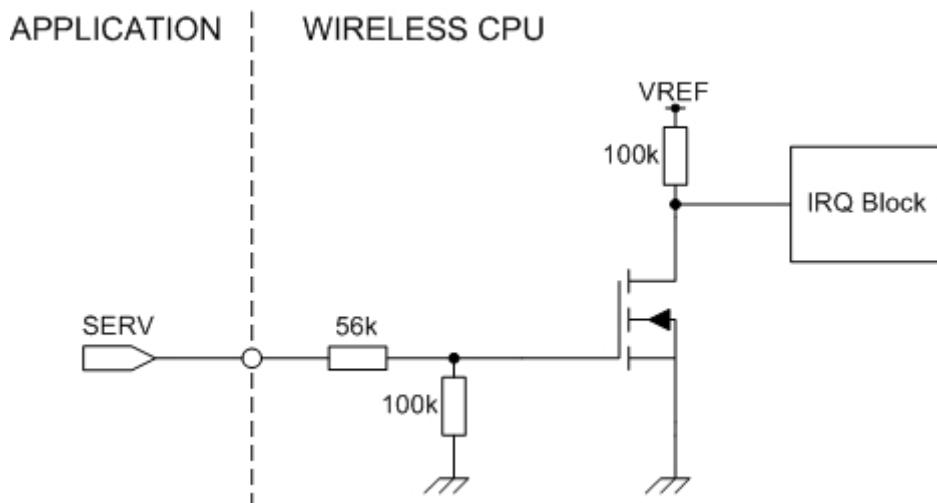
Figure 24: SERVICE Pin Interface

Signal	Mode		Value	Unit
SERVICE	Active High	Minimum input voltage	2.5	V
		Maximum input voltage	12.0	V
	Inactive Low	Maximum input voltage	0.8	V

	The application must have the capability to set this signal active high. The signal is not needed to perform normal SW–updating through "Updater", but it is needed to support special service tools from Wavecom.
CAUTION	

	The SW updating tool for GR64 is "Updater". The Updater is a local application that downloads a signed image provided by Wavecom. It is not necessary to set SERV active to run "Updater".
NOTE	

4.14 Buzzer

Pin	Name	Direction	Function
31	BUZZER	Output	Buzzer Output

Connecting the BUZZER signal to an inverting transistor–buffer followed by a piezoelectric transducer enables the Wireless CPU® to play pre–programmed melodies or sounds. A recommended implementation is shown below.
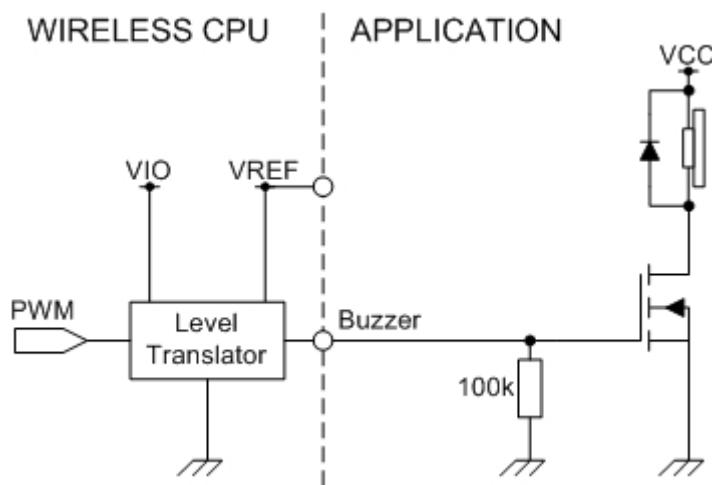
Figure 25: Recommended circuit for a Buzzer implementation

4.15 LED

Pin	Name	Direction	Function
33	LED	Output	LED control signal

The LED interface is intended to operate a status LED, which can be programmed on and off, or for a particular blink sequence. The LED signal is derived from a standard GPIO and does not have sufficient drive capability to operate an LED directly, so it requires the user to implement some form of transistor circuit. A recommended implementation is shown below.
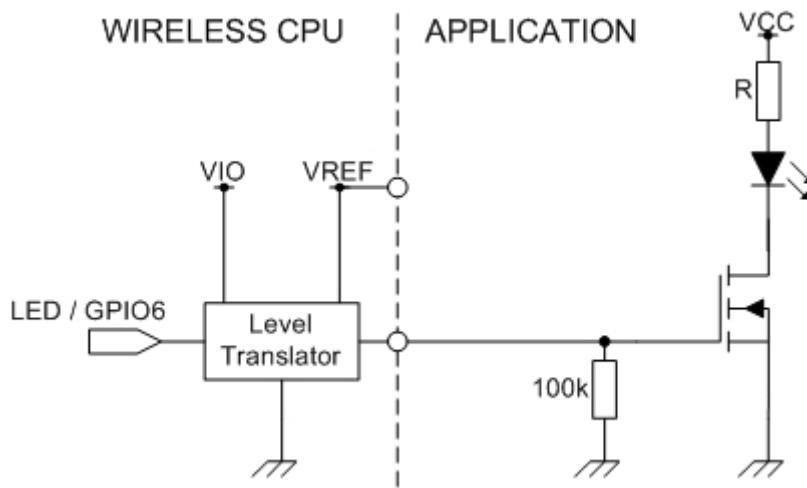
Figure 26: Recommended circuit for an LED implementation

4.16 General Purpose IO

Pin	Name	Default	Alternate function
21	GPIO1	GPIO1	
22	GPIO2	GPIO2	
23	GPIO3	GPIO3	
24	GPIO4	GPIO4	
13	GPIO5	ADIN4	ADC Input 4
33	GPIO6	LED	LED control signal
32	GPIO7	DSR1	Data Set Ready (UART1)
36	GPIO8	RI	Ring Indicator
39	GPIO9	RTS1	Ready To Send (UART1)
37	GPIO10	DTR1	Data Terminal Ready (UART1)
38	GPIO11	DCD1	Data Carrier Detect (UART1)
40	GPIO12	CTS1	Clear To Send (UART1)
29	GPIO13	SDA	GPIO13
30	GPIO14	SCL	GPIO14
20	GPIO15	GPIO15	

All general purpose IO (GPIO) is programmable by the user. Some GPIO has alternate functionality already associated with it; this is indicated in the default column. GPIO which has alternate function is effectively multiplexed, so that the user chooses through AT commands the appropriate configuration for their application.

GPIO is programmable for the following features:

- An input or output
- Level-sensitive or transition-sensitive

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- Polarity (inversion)
- Internal pull-up resistors

CAUTION

The internal pull-up resistors are applied on the Wireless CPU® side of the level translators. If the application is using a GPIO as an input and need a pull-up resistor, the application must provide that externally. To overcome the 6k input impedance of the level translator, the pull-up resistor must be in the 680 ohm range. This could potentially increase current consumption, so it is recommended to use CMOS-logic (see 4.3.1.1 for more information).

It is recommended to use the GPIO's as direct drive with internal pull-up resistors disabled.

If pins labelled in the table above are not being used for the indicated alternative function they may be used as general purpose inputs or outputs; they are not constrained to work in only one direction. All GPIO is level shifted on the GR64, and has the characteristics defined in section 4.3.

GPIO has a number of sharing (configuration) options. Sharing means that it is not feasible to operate all the alternative features concurrently, however, with care, dynamic switching from one feature to another is possible.

Users should note that if flow control is required for UART1 then GPIOs 7 to 12 inclusive cannot be configured for general purpose use.

Some GPIO is configured to provide a keyboard interface (details are covered in the next section).

4.16.1 Embedded Applications

When a particular IO feature is required, the user sets the state of the relevant IO blocks by disabling one set before enabling others.

The Wireless CPU® checks the state of the IO when the user requests a new function. The new function is rejected if the current function is not released first.

The states of GPIOn to GPIOm are retained for the next power up. For example, inputs remain as inputs and outputs remain as outputs. The voltage of a defined output pin will still drop to 0 Volts in the Wireless CPU® power down state.

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4.16.2 LED/IO6 Capabilities

The LED function pin can be used as a general purpose digital I/O when the flashing LED function is not required. However, this pin does not have an on-board pull-up resistor. It is required that an external pull-up or pull-down resistor be provided by the host circuitry when either not used or when used as a digital input.

4.16.3 ADIN4

A further ADC input (in addition to the three dedicated pins) is created by multiplexing one of the GPIO signals (GPIO5).

4.17 Analogue to Digital Converters (ADIN1, ADIN2, ADIN3, ADIN4)

Pin	Name	Direction	Function
26	ADIN1	Input	ADC Input 1
27	ADIN2	Input	ADC Input 2
28	ADIN3	Input	ADC Input 3
13	ADIN4	Input	ADC Input 4 /GPIO5

ADC pins is converted and stored in a register inside the Wireless CPU®. When the appropriate AT command is received by the Wireless CPU®, the digital value stored in the register is read.

The Wireless CPU® has a single precision 10-bit ADC, shared by a number of functions within the Wireless CPU® and also through the external interface connections (three dedicated, one shared). The ADC sharing arrangement is shown below.
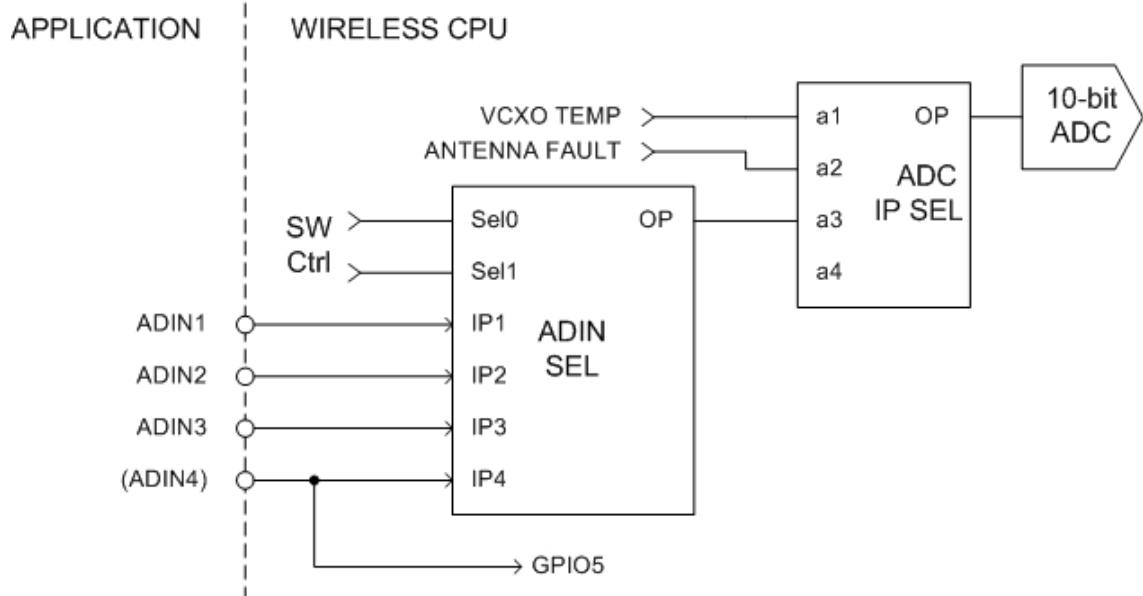
Figure 27: ADC sharing arrangement

ADC sampling frequency and sampling source selection can be set up and controlled with AT-commands by the user. ADC samples requires up to 5 clock (ADCLK) cycles to process. The ADC also performs some system-level sampling. These two factors limit the maximum practical sampling rate to around 20ksps.

Parameter	Condition	Min	Typ	Max	Unit
Resolution			10		bit
Coding: Unsigned Magnitude		000		3FF	Hex
Differential Nonlinearity		-1		1	lsb
Integral Nonlinearity		-10		10	lsb
Full-scale Error		-3		3	%
Offset Error		-14		14	lsb
Conversion Gain*			421		lsb/V
Conversion Intercept*			-9		lsb
Low-level Input Voltage	ADC output=000h				

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High-level Input Voltage	ADC output=3FFh	2.45		2.59	V
ADC Clock (ADCLK)		260	325	390	kHz
ADC Conversion Time			12		ADCLK
ADC Sample Delay				5	ADCLK

4.18 I2C Serial Control Bus

Pin	Name	Direction	Function
29	SDA	In/Out	I2C data
30	SCL	Output	I2C clock

The I2C interface comprises two signals; data (SDA) and clock (SCL). Both SDA and SCL have pull-up resistors. Therefore, when the bus is free, both SDA and SCL are in a HIGH state.

The GR64 implementation of I2C supports only a single master mode, with the Wireless CPU® being the master. The output stages of SDA and SCL must have an open-drain or open-collector to perform a wired-AND function. The wired-AND function provides the I2C bus ability to perform clock synchronization on the SCL line. Due to the wired-AND function, the SCL line will be held LOW by the device with the longest LOW period. Therefore, the device with the shorter LOW period will be in a HIGH wait-state during this time.

Clock synchronization can be used as a handshaking mechanism, to enable receivers to cope with fast data transfers. On a byte level, a slave (host application-side) I2C device may be able receive a data transfer, but need time to store the byte received before it is ready to receive another byte. The slave/receiver will therefore hold the SCL line low, after sending the acknowledge bit following the byte received, thereby forcing the master into a wait state. Once the SCL is released by the slave/receiver, the wait state of the master will end. This feature of the I2C standard is known as clock-stretching and is supported by the GR64.

The I2C interface supports Standard-mode (100kbps) and Fast-mode (400kbps). It also supports Normal (7-bit) addressing and extended (10-bit) addressing.

TIP

The SDA and SCL pins can be set as GPIO, as noted in the table in section 4.16 on page 73. Please see the AT*E2I2C command in the AT Commands Manual for more details.

Fast-mode signal characteristics

Parameter	Min	Typ	Max	Unit
SCL clock frequency	0		400	kHz
LOW period of the SCL clock	1.3			µs
HIGH period of the SCL clock	0.6			µs
Data hold time	0		0.9	µs
Capacitive load for each bus line			400	pF

4.19 Burst Transmission (TX_ON)

Pin	Name	Direction	Function
35	TX_ON	Output	Transmit indication

Burst transmission is the period during which the GSM transceiver is transmitting RF signals. TX_ON is an indicator that the Wireless CPU® is transmitting.

A typical application may use TX_ON to blank adjacent receiver circuitry as a means of protecting sensitive input stages. TX_ON is active HIGH.

TX_ON characteristics

| Parameter	Condition	Min	Typ	Max	Unit
Output Voltage High (VOH)	IL = 80uA	2.0	2.8	3.0	V
Output Voltage low (VOL)	IL = 80uA			1.0	V

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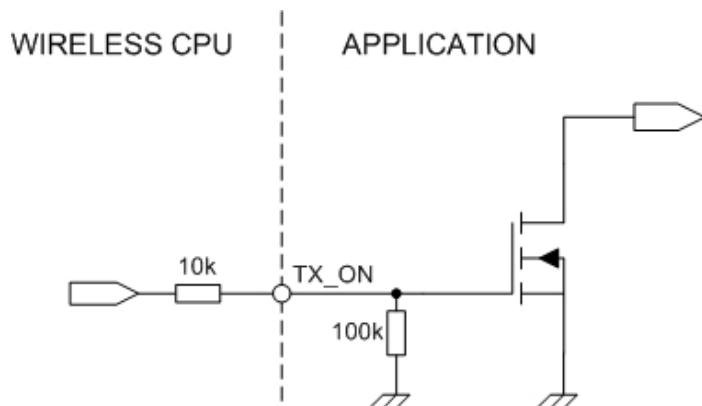
Figure 28: Recommended circuitry for a TX_ON implementation

4.20 Real Time Clock

The real-time clock (RTC) is driven by a 32.768 kHz clock from an internal crystal oscillator. The clock is divided by 32,768 to generate a clock with a 1 second period that increments a 29-bit seconds counter. In addition, it can generate interrupts at a programmed time. The following are the features of RTC:

- 17-year time interval with 1 second resolution.
- Programmed time alarm interrupt
- Alarm output pin

An RTC alarm can be set by loading an appropriate value into the seconds alarm register and enabling an interrupt via an AT-command.

The RTC relies on an uninterrupted 1.5 V (nominal) power supply (VRTC), whether the Wireless CPU® is powered off or on. The RTC-alarm operates from the VRTC supply, and therefore utilizes a 1.5 V logic level. Users have the responsibility to provide a backup battery to provide uninterrupted VRTC function when the Wireless CPU® is powered down.

Parameter	Condition	Min	Typ	Max	Unit
RTC accuracy	Ambient (+25±2°C) operation			52.6	Secs/month
RTC accuracy	Extreme temperatures			65.2	Secs/month
VRTC	RTC Operational supply voltage range	1.10	1.50	1.65	V

4.20.1 Real Time Clock Backup Supply (VRTC)

Pin	Name	Direction	Function
25	VRTC	Input	DC supply for real time clock

VRTC provides an input connection to the Wireless CPU® which allows the user to power the real time clock (RTC) within the GR64 by way of a coin cell or charged capacitor.

When the Wireless CPU® is powered, an internal LDO regulator provides a 200 A source designed to supply the microprocessor's RTC block. It is also intended to recondition a rechargeable coin cell that supplies the RTC Wireless CPU® when the main battery is removed, or has insufficient energy. Because this LDO is always on, even when the Wireless CPU® is powered down, it features very low quiescent current. It also offers reverse current protection, with low leakage, when the coin cell is powering the RTC block.

The RTC LDO is primarily designed to charge manganese–silicon lithium batteries. Rechargeable coin cells with different chemical composition may also be charged provided their charging requirements are consistent with the RTC LDO's electrical characteristics. The VRTC output is nominally 1.5 V.

VRTC LDO characteristics:

Parameter	Condition	Min	Typ	Max	Unit
Output Voltage Tolerance	IOUT = 10 µA	1.35	1.50	1.65	V
Maximum Output Current		200			µA
Short–circuit Current Limit	VRTC to GND	0.7	1.6	2.9	mA
Output Resistance	IOUT = 10 µA	75	100	150	ohm
Line Regulation	IOUT = 10 µA			5	mV
Off Reverse Leakage Current			0.1	1	µA

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In the backup condition the RTC block will function to as low as 1.1V on the VRTC pin. The RTC draws 10µA typically during powered backup (15µA max).

Figure 29 shows the VRTC connectivity arrangement.
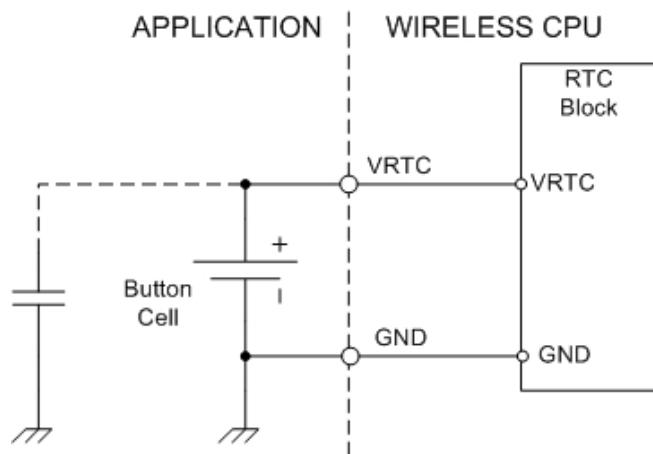

Figure 29: VRTC connection

Recommended button cell to use is Seiko TS414H. This is a lead-free, reflowable SMT Lithium battery with a nominal voltage of 1.5V.

TIP

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4.20.2 RTC Alarm (ALARM)

Pin	Name	Direction	Function
50	ALARM	Output	RTC Alarm

NOTE	The ALARM signal is only available on GR64002.

The Alarm output is logic output from the Wireless CPU® which is supplied from the RTC circuitry block. This block is, in turn, supplied either from the main supply of the Wireless CPU® or from a backup battery if the main supply is not available.

This signal is pulled up inside the Wireless CPU® to VRTC and is set low for 1s when an Alarm is triggered.

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5 Antenna Connector

The Wireless CPU®'s antenna connector allows transmission of the radio frequency (RF) signals from the Wireless CPU® to an external customer supplied antenna. The connector is a micro-miniature coaxial MMCX through hole-mounted socket. A number of suitable MMCX type, mating plugs are available from the following manufacturers:

- Amphenol
- Suhner
- IMS Connector Systems

The nominal impedance of the antenna interface is 50 ohms.

Feature	GSM850	E-GSM900	GSM1800	GSM1900
Frequency range (MHz)	824–894	880–960	1710–1880	1850–1990
Maximum power	33dBm (2W)	33dBm (2W)	30dBm (1W)	30dBm (1W)
Antenna Connector impedance	50 ohms			
Antenna VSWR	2.5:1 operating max			

NOTE

To bypass the MMCX connector, two PCB landing pads are available on the underside of the Wireless CPU®. The integrator can probe these pads or solder a coaxial cable directly to them. Wavecom; however, cannot guarantee absolute performance when connecting to the antenna in this way due to the attenuation such a connection could potentially cause. When connecting in this way, proceed with care.
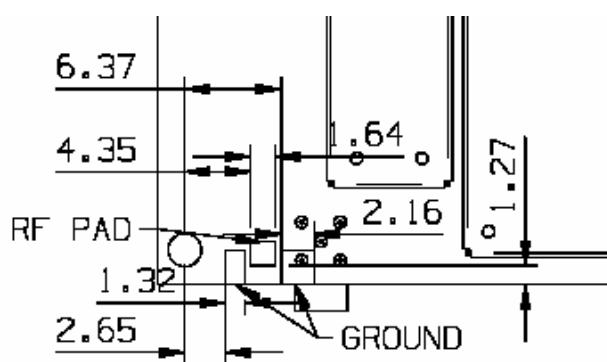

Figure 30: RF Antenna Pad Dimensions

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6 Hints for Integrating the Wireless CPU®

This chapter gives the integrator advice and helpful hints on how to integrate the Wireless CPU® into the application from a hardware perspective.

Make sure the integrator read and consider the information under the following headings before starting the integration work:

- Safety advice and precautions
- Installation of the Wireless CPU®
- Antenna

6.1 Safety Advice and Precautions

6.1.1 General

Always ensure that use of the Wireless CPU® is permitted. The radio device may present a hazard if used in proximity to personal medical electronic devices. As a rule, the Wireless CPU® must not be used in hospitals or onboard aircraft.

The integrator are responsible for observing the country's safety standards, and where applicable, the relevant wiring rules.

Never use the Wireless CPU® at a gas station refuelling point, blasting area or in any other environment where combustible vapours or explosives may be present.

Operating the Wireless CPU® close to other electronic devices, such as antennas, television sets, and radios may cause electromagnetic interference.

Never try to dismantle the Wireless CPU® yourself. There are no components inside the Wireless CPU® that can be serviced by the user. Dismantling the Wireless CPU® may invalidate the warranty.

To protect the power supply cables and meet the fire safety requirements, it is recommended that the electrical circuits are supplied with a power regulator. The power regulator should be placed as close to the terminals of the power supply as possible.

Do not connect any incompatible component or product to the Wireless CPU®.

⚠ WARNING	Wavecom does not warrant against defects, malfunction, non-conformities or deviation caused by the connection of incompatible components or products to the GR64.

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6.2   SIM Card

Before handling any SIM card, users should ensure that they are not charged with static electricity.   Use proper precautions to avoid electrostatic discharges. The Wireless CPU® must be switched off before the SIM card is installed or uninstalled.

When the SIM card holder is opened, the SIM card connections lie exposed under the SIM card holder.

CAUTION: Do not touch these connections! Failure to heed this advice may release an electrical discharge that could damage the Wireless CPU® or the SIM card.

When designing applications, the SIM card's accessibility should be taken into account.   Wavecom recommends that users protect SIM card access by a PIN code. This will ensure that the SIM card cannot be used by an unauthorized person.

6.3   Antenna

If the antenna is to be mounted outside, consider the risk of lightning.

Always follow the instructions provided by the antenna manufacturer.

Never connect more than one Wireless CPU® to a single antenna.

The Wireless CPU® can be damaged by radio frequency energy from the transmitter of another adjacent wireless transmitter.

Like any Wireless CPU®, the antenna of the Wireless CPU® emits radio frequency energy.   To avoid EMI (electromagnetic interference), users must determine whether the application itself, or equipment in the application's proximity, requires further protection against radio emission and the disturbances it might cause. Protection is secured either by shielding the surrounding electronics or by moving the antenna away from the electronics and the external signals cable.

The Wireless CPU® and antenna may be damaged if either come into contact with ground potentials other than the one in the user's application.   Beware, ground potential are not always what they appear to be.

In the final application, the antenna must be positioned more than 20 cm away from human bodies.   When this rule cannot be applied, the application designer is responsible for providing the SAR measurement test report and declaration.

Even if SAR measurements are not required, it is considered good practice to insert a warning in any manual produced, indicating it is a radio product and that care should be taken.

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6.4 Installation of the Wireless CPU®

6.4.1 Where to Install the Wireless CPU®

The following conditions need to be taken into consideration when designing the application as they might affect the Wireless CPU® and its function:

- Environmental conditions
- Signal strength
- Connection of components to Wireless CPU®
- Network and subscription

6.4.1.1 Environmental Conditions

The Wireless CPU® must be installed so that the environmental conditions stated in the Technical Data chapter, such as temperature, humidity and vibration are satisfied. Additionally, the electrical specifications in the Technical Data section must not be exceeded.

6.4.1.2 Signal Strength

The Wireless CPU® has to be placed in a way that ensures sufficient signal strength. To improve signal strength, the antenna can be moved to another position. Signal strength may depend on how close the Wireless CPU® is to a radio base station. The integrator must ensure that the intended usage location is within the network coverage area.

Degradation in signal strength can be the result of a disturbance from another source, for example an electronic device in the immediate vicinity. More information about possible communication disturbances can be found in section 8.3.5, page 59.

When an application is completed, the integrator can verify signal strength by issuing the AT command AT+CSQ or AT*E2EMM. See the AT Commands Manual for further details.
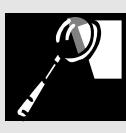
| TIP | Before installing the Wireless CPU®, use an ordinary mobile telephone to check a possible location for it. In determining the location for the radio device and antenna, the integrator should consider signal strength as well as cable length. |

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6.4.1.3   Connection of Components to Wireless CPU®

The integrator is responsible for the final integrated system. Incorrectly designed or installed, external components may cause radiation limits to be exceeded. For instance, improperly made connections or improperly installed antennas can disturb the network and lead to malfunctions in the Wireless CPU® or equipment.

6.4.1.4   Network and Subscription

Before the integrator's application is used, the user must ensure that their chosen network provides the necessary telecommunication services. Integrators should contact their service provider to obtain the necessary information.

Integrators intending to use SMS in the application should ensure this is included in their (voice) subscription.

Similarly, integrators intending to use GPRS for data services should also ensure that this service is available on their network and in their account plan.

Users should consider the choice of the supplementary services described in section 2.3.2 Short Message Service.

6.4.2   How to Install the Wireless CPU®

6.4.2.1   Power Supply

Use a high–quality power supply cable with low resistance. This ensures that the voltages at the connector pins are within the allowed range, even during the maximum peak current. An electrolytic capacitor should be placed close to the power supply pins of the Wireless CPU® to supply the peak currents during burst transmission. See 4.5 Regulated Power Supply Input (VCC).

6.4.2.2   Grounds

A ground connection is provided at the mounting hole next to the RF connector on the Wireless CPU® (see Figure 8, page 30). Connect this ground point to the GND pins of the Wireless CPU® by the shortest, low impedance path possible. The purpose of this connection is to allow any ESD picked up by the antenna to bypass the Wireless CPU®'s internal ground path.

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NOTE	It is recommended that the integrator use a cable with a maximum resistance of 5 milli ohm for the ground connection. AREF and GND are connected at a single point inside the Wireless CPU®. They must not be joined together in the application.

6.4.2.3   Audio

Use coupling capacitors on MICIP / MICIN lines if the application does not use the Wireless CPU®'s bias voltage. See also 4.9.3 Microphone Signals (MICIP, MICIN).

6.4.2.4   Software Upgrade

There is one way of updating the firmware in the GR64. This is an Updater, which is a local application that downloads an image provided by Wavecom.

6.5   Antenna

6.5.1   General

The antenna is the component in the users system that maintains the radio link between the network and the Wireless CPU®. Since the antenna transmits and receives electromagnetic energy, its efficient function will depend on:

- Type of antenna (for example, circular or directional)
- Placement of the antenna
- Communication disturbances in the vicinity in which the antenna operates

In the sections below, issues concerning antenna type, antenna placement, antenna cable, and possible communication disturbances are addressed.

In any event, users should contact their local antenna manufacturer for additional information concerning antenna type, cables, connectors, antenna placement, and the surrounding area. Users should also determine whether the antenna needs to be grounded or not. Usually, a local antenna manufacturer should be able to design a special antenna suitable for the integrators application and environment.

6.5.2 Antenna Type

Users should ensure that they choose the right type of antenna for the Wireless CPU®.

The antenna must be designed for the frequency bands deployed in the regions that the Wireless CPU® is being used. For fixed locations this may be dual bands (for example E-GSM900/GSM1800 in Europe; GSM850/GSM1900 in North America). For applications which are mobile, users should consider whether three or all four GSM bands could be encountered.

Other factors in choosing antenna are equally important:

· Impedance of the antenna and antenna cable must be 50 ohms at all frequencies being used.

· Antenna output-power handling capability must be a minimum of 2 W.

· Antenna VSWR value should be less than 3:1 to avoid damage to the radio device.

6.5.3 Antenna Placement

The antenna should be placed away from electronic devices or other antennas. The recommended minimum distance between adjacent antennas, operating in a similar radio frequency band, is at least 50 cm.

If signal strength is weak, it is useful to face a directional antenna at the closest radio base station. This can increase the strength of the signal received by the Wireless CPU®.

The Wireless CPU®'s peak output power can reach 2 W. RF field strength varies with antenna type and distance. At 10 cm from the antenna the field strength may be up to 70 V/m and at 1m it will have reduced to 7 V/m.

In general, CE-marked products for residential and commercial areas, and light industry can withstand a minimum of 3 V/m.

6.5.4 The Antenna Cable

Use 50 ohm impedance low-loss cable and high-quality 50 ohm impedance connectors (frequency range up to at least 2 GHz) to avoid RF losses. Ensure that the antenna cable is as short as possible.

The effectiveness of the antenna, cable and connectors is determined by their quality. All connectors, adaptors and cables should be of the highest quality, lowest loss, lowest VSWR rating that is affordable to the user.

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Minimize the use of extension cables, connectors and adapters. Each additional cable, connector or adapter will result in additional loss of signal power.

6.5.5 Possible Communication Disturbances

Communication disturbances can adversely affect the quality of wireless links, including the following causes:

- Noise can be caused by electronic devices and radio transmitters.

- Path-loss occurs as the strength of the received signal steadily decreases in proportion to the distance from the transmitter.

- Shadowing is a form of environmental attenuation of radio signals caused by hills, buildings, trees or even vehicles. This can be a particular problem inside buildings, especially if the walls are thick and reinforced.

- Multi-path fading is a sudden decrease or increase in the signal strength. This is the result of interference caused when direct and reflected signals reach the antenna simultaneously. Surfaces such as buildings, streets, vehicles, etc., can reflect signals.

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7 Embedded Applications

The Wireless CPU® has the capability to store and run customer written code in the form of a script during the processor's idle time, through the use of an on board interpreter.

7.1 Features

Main features of embedded applications are as follows:

- C-based scripting language (Wavecom specific)
- Over the air upgrade of scripts (scripts only, NOT GSM software)
- Library of intrinsic functions
- 2 scripts can be stored in the memory at any time (but only 1 can be active/running)

7.2 Implementation

The Wireless CPU® has 2x124KB of non volatile memory space available for storage of two scripts in the scripting language. The maximum size of a single script is 124K, regardless of the size/presence of the other script. 224KB of RAM is set aside for the script usage. Since the script is loaded from non volatile memory into this RAM portion, the RAM available for the script to use for variables is 224KB - size of the script.

Structures included in this language are:

- If - else statements
- While loops
- For loops

All hardware interfaces that are normally available to the Wireless CPU® through the AT commands, are also available to the embedded application.

Further drivers have been written such as M bus, keypad, SPI and I2C for use by the embedded application (EA) through the use of the I/O pins.

7.2.1   Limitations

Since the Wireless CPU® is processing the script using its own memory, limitations are placed onto the scripts that are run.

A direct comparison cannot be made to a fully compiled C program in terms of size, but a gauge of script size is that if each line were 64 characters long (not counting comments or any form of white space) in the script then the script could be about 2000 lines long.

Processing power is something that needs to be considered as the script is run as a low priority process within the software. However, controller mode stops GSM operation and provides all the processing power for the script to be run. See the M2mpower Application Guide for more details.

Code cannot be ported directly from an existing application and loaded directly onto the Wireless CPU®. It must be re-written in the Wavecom Mobile script language so that the Wireless CPU® interpreter can function correctly.

7.2.2   M2mpower IDE (Integrated Development Environment)

The IDE is a Windows based package which allows the user to write, simulate, debug and download the application into a Wireless CPU® with the embedded application (EA) software. The standard version is designed to run on Windows XP and 2000.

The M2mpower Application Guide is available for implementing applications using the developer's kit and the embedded application (EA) functionality.

This is a required package to be able to implement an embedded application (EA).

For further information please contact Wavecom Mobile Communications customer support.

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8 TCP/IP Stack

An on board IP/TCP/UDP stack has been integrated into the software negating the need for the customer to implement one in their own code base.

This is accessible by using an embedded application (see section 9) using intrinsic functions.

8.1 Implementation

The following types of commands allow various functions:

- Open/closing IP connections – Negotiates/closes an IP address with the web server.

- Send/Receive TCP packets – Performs all TCP operations to send and receive packets.

- Send/Receive UDP packets – Performs all UDP operations to send and receive packets.

- Resolve URL to an IP address – Similar to nslookup command in DOS When the unit is set up and controlled using the embedded applications.

- The embedded applications or an external application can generate data to be sent and pass it to the Wireless CPU® for transmission.

This effectively provides a transparent communication link from the application to an internet server over GPRS.

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9 Technical Data

9.1 Mechanical Specifications

Refer to Figure 3 & Figure 4 for reference to mechanical features.

| Mechanical Feature	Variant	Value
Length		50 mm
Width		33 mm
Thickness (see illustration below)	without SIM holder	3.3 mm
	with SIM holder	5.9 mm
Weight	without SIM holder	8 grams
	with SIM holder	9 grams

3.3
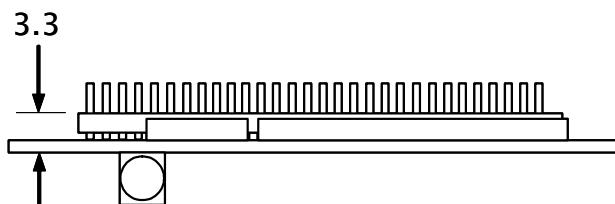
Figure 31: Thickness of Wireless CPU® variant without SIM holder

5.9
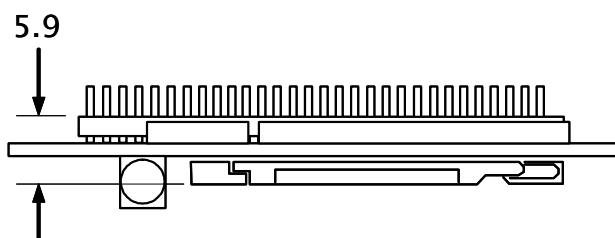
Figure 32: Thickness of Wireless CPU® variant with SIM holder

9.2 Power supply voltage, normal operation

Parameter	Mode	Limit
VCC Supply voltage	Nominal	3.6 V
	Min	3.2 V
	Max	4.5 V
	Absolute maximum voltage range	–0.3 to 6.5 V
	Maximum supply ripple	<100mV @ <200kHz <20mV @ >200kHz
Maximum allowable voltage drop	Transmission burst	200mV
Maximum current consumed	Full power (2W) transmit	2250 mA (peak) 2100 mA (average)

WARNING

Stresses in excess of the absolute maximum limits can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the normal Min & Max values stated. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

9.3 Radio specifications

Feature	GSM850	E–GSM900	GSM1800	GSM1900
Frequency range (MHz)	824–894	880–960	1710–1880	1850–1990
Maximum power	33dBm (2W)	33dBm (2W)	30dBm (1W)	30dBm (1W)
Antenna impedance	50 ohms			

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9.4   SIM card

Parameter	1.8V	3.0V	5.0V
External SIM support	Yes	Yes	No
Integrated SIM support (optional)	Yes	Yes	No

9.5   Environmental Specification

Table 6: Environmental Test cases

Test Case	Test Summary	Ref Standard
Heat Test	Temp: max storage Humidity: nominal Duration: 16 hours	IEC 60068–2–2
Cold Test	Temp: min storage Duration: 16 hours	IEC 60068–2–1
Temperature Cycling	Temp (low) : min storage Temp (high) : max storage 2 hrs dwell at each extreme 6 hrs transition between temps Duration: 5 cycles x 16 hours (80 hrs total)	IEC 60068–2–14

Test Case	Test Summary	Ref Standard
Thermal Shock Test	Temp (low) : min storage Temp (high) : max storage 6 min dwell at each extreme 0.5 to 3 min transition Duration: 30 cycles (Group 2,3)	IEC 60068-2-14
Moist Heat Cyclic Test	Temp (low) : nominal ambient Temp (high) : max operating Humidity (high) : 95% ±5% RH 9 hr dwell at each temperature 3 hr transition between temps Duration: 6 cycles x 24 hours (144 hrs total)	IEC 60068-2-30
Operational Durability	SIM insertion : 500 cycles System connector : 10,000 cycles RF connector : 5,000	1/52 41-FEA 202 8370
Free Fall Test	1m drop height on to concrete – all sides – all faces – all corners – any extended features	IEC 60068-2-32 Test Ed

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Test Case	Test Summary	Ref Standard
Sinusoidal Vibration	Freq: 10-60 Hz, constant displacement $\equiv \pm 0.35mm$ Freq : 60-500 Hz, constant acceleration $\equiv$ 5 g Sweep velocity: 1 oct/min Sweeps: 5 per axis Axis: 3 axis (x, y, z) per device	IEC 60068-2-6
Random Vibration	Power Spectral Density: 5 Hz 0.10 m^2/s^3 12 Hz 2.20 m^2/s^3 20 Hz 2.20 m^2/s^3 200 Hz 0.04 m^2/s^3 500 Hz 0.04 m^2/s^3 Duration : 2 hrs each axis Axis : 3 axis (x, y, z) per device	IEC 60068-2-34
Mechanical Shock Test	Pulse shape: Half-sine Amplitude: 30 g$\pm$15% Duration: 6 ms Axis: $\pm$x, $\pm$y, $\pm$z No. shocks: 3 each direction (18 total)	IEC 60068-2-27 Test Ea
Mixed Plug-in Connector	Mechanical force : 50 N in $\pm$x, -y, $\pm$z directions 100 N in +y (mating axis)	1/152 41-FEA 202 8370

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10   Regulatory Notices

CE

The GR64 described in this manual conforms to the Radio and Telecommunications Terminal Equipment (R&TTE) directive 99/5/EC with requirements covering EMC directive 89/336/EEC and Low Voltage directive 73/23/EEC. The product fulfils the requirements according to 3GPP TS 51.010-1, EN 301 489-7 and EN60950.

This device complies with Part 15 of the FCC rules. Operation is subject to the following two conditions:

(1) This device may not cause harmful interference, and

(2) The device must accept any interference received, including interference that may cause undesired operation.

The GR64 modular transmitter is labelled with its own FCC ID number. In the normal method of mounting the GR64 in a customer application the label is not visible to an end-user. Similarly, the customer application itself may obscure the GR64 Wireless CPU® entirely. If the FCC ID is not visible when the Wireless CPU® is installed inside another device, then the outside of the device into which the Wireless CPU® is installed must display a label referring to the enclosed Wireless CPU®. This exterior label can use wording such as the following: "Contains Transmitter Wireless CPU® FCC ID: PY7BC051021" or "Contains FCC ID: PY7BC051021". Any similar wording that expresses the same meaning may be used.

FCC ID PY7BC051021	The GR64 product has received GCF and FCC approval
IC: 4170B–BC051021	

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GRANT OF EQUIPMENT
AUTHORIZATION

Certification
Issued Under the Authority of the
Federal Communications Commission
By:

CKC Certification Services
5046 Sierra Pines
Mariposa, CA 95338

Date of Grant: 08/22/2006

Application Dated: 05/22/2006

Sony Ericsson Mobile Communications AB
Nya Vattentornet
Lund, 22188
Sweden

Attention: Mats Hansson , Senior Staff Engineer

NOT TRANSFERABLE

EQUIPMENT AUTHORIZATION is hereby issued to the named GRANTEE, and
is VALID ONLY for the equipment identified hereon for use under the
Commission's Rules and Regulations listed below.

FCC IDENTIFIER: PY7BC051021
Name of Grantee: Sony Ericsson Mobile Communications AB
Equipment Class: PCS Licensed Transmitter
Notes: Quadband GPRS Module

Grant Notes	FCC Rule Parts	Frequency Range (MHZ)	Output Watts	Frequency Tolerance	Emission Designator
	24E	1850.2 - 1908.8	0.440	0.022 PM	GXW
	22H	824.2 - 848.8	0.773	0.018 PM	GXW

Modular Approval. Output power is ERP for Part 22 and EIRP for Part 24. This device
contains 900MHz and 1800 MHz functions that are not operational in U.S. Territories.
Compliance of this device in all final host configurations is the responsibility of the
Grantee. This device is approved for mobile RF exposure conditions. Approved for use
with antenna(s) as listed in this filing. The antenna(s) used for this transmitter must be
installed to provide a separation distance of at least 20 cm from all persons and must
not be co-located or operating in conjunction with any other antenna or transmitter.
OEM integrators must be provided with antenna installation instructions. OEM
integrators and end-Users must be provided with transmitter operation conditions for
satisfying RF exposure compliance. This grant is valid only when the device is sold to
OEM integrators and the OEM integrators are instructed to ensure that the end user
has no manual instructions to remove or install the device.

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Make it wireless
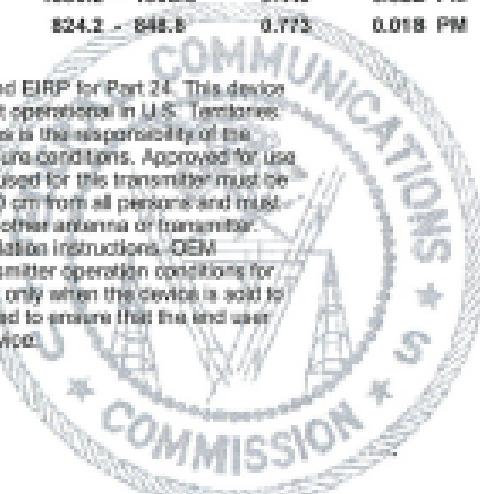
CERTIFICATION BODY
CERTIFICATE OF COMPLIANCE

ISSUED UNDER THE AUTHORITY OF MINISTER OF INDUSTRY

Presented by:
CKC Certification Services
4933 Sierra Pines Drive
Mariposa, CA 95338

Certificate Issued to:

Certificate Holder: **Sony Ericsson Mobile Communications AB**
Nya Vattentornet
Lund 22188
Sweden
Phone: 44 7808944467
Company Number: 4170B

Specifications Certified:

Specification: RSS 132   Issue   2
RSS-133   Issue   3
Amendment(s):
Date of Issue: RSS-132 September 2005
RSS-133 June 2005

Product Identification:

Certification Number: 4170B-BC051021
Model or Trade Name: **GR64**
Application ID: E06-000153
Type of Equipment: Cellular Mobile GSM (824-849 MHz)
PCS Mobile (1850-1910 MHz)
Application Purpose: Original / New

Operational Summary:

Type of Transmission: Data
Type(s) of Modulation: GMSK
Signal Information: GSM
Antenna Information: External

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Make it wireless

CERTIFICATION BODY
CERTIFICATE OF COMPLIANCE

Equipment Specifications: RSS-132

Frequency Range (MHz)	Carrier Output (Watts) (dBµV/m @ X m)	99% Bandwidth (kHz)	Emission Type(s)	Transmitter Field Strength of Spurious Radiation (Worst Case) Indicate Units (dBµ)	Receiver Field Strength of Spurious Radiation (Worst Case) Indicate Units dBuV/m @ 3m
824.2-848.8	0.733	279	GXW	73.9	27.2

Equipment Specifications: RSS-133

1850.2-1909.8	0.449	283	GXW	63.0	28.25

Test Laboratory:

Test Laboratory: CETECOM Inc.
411 Dixon Landing Road
Milpitas, CA 95035
408-586-6200

OATS Listing: 3925A

Certification of equipment means only that the equipment has met the requirements of the above noted specification. License applications, where applicable to use certified equipment, are acted on accordingly by the issuing office and will depend on the existing radio environment, service and location of operation. This certificate is issued on condition that the holder complies and will continue to comply with requirements and procedures issued by Industry Canada.

Acceptance Date: May 22, 2006

CKCCS Committee Chairman

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DEVELOPERS KIT

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# 11 Introduction to the Universal Developer's Kit

The Wavecom universal developer's kit (UDK) is designed to get the integrator started quickly. It contains all the hardware the integrator will need to begin the development of an application.

The only items the integrator needs to provide are; a Wireless CPU®, a computer, a SIM card with a network subscription, and knowledge of programming with AT commands.

The main hardware of the UDK is an open board onto which the integrator plugs the Wireless CPU®, using an adaptor board where necessary. Connectors, switches, jumpers and SIM card holder are provided to allow the integrator to configure and access all the functions of the radio device.

Two version of the UDK exists; the first-generation UDK is designed for legacy M2M products available during 2003 to 2005; a second-generation Universal Developers Kit Mk 2 is available for M2M products from 2006 onwards. Components, adaptor boards and peripheral interfaces are not inter-changeable between the two UDK products.

A separate user manual describes the set-up and use of the UDK. This can be downloaded from the Wavecom M2M Extranet web pages or obtained from the local sales support representative upon request.

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